Universidad de Oviedo

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Técnica Industrial de Gijón

Proyecto de Fin de Carrera

Microbot con Sensores de Ultrasonidos Controlado por Microcontrolador

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Hecho con $\LaTeX$

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Capítulo 1
Introducción

1.1. Objetivo

El presente proyecto tiene como objetivo la construcción de un microbot, y la realización practica de un prototipo.

El microbot debe cumplir una serie de condiciones:

- Pequeño tamaño, y capacidad de movimiento autónomo.
- Estará controlado por un Microcontrolador.
- Dispone de varios sensores de Ultrasonidos, y sera capaz de detectar obstáculos y evitarlos.

A lo largo del proyecto se analizaran las diferentes opciones posibles para su desarrollo.

1.2. Robots

La palabra robot tiene sus orígenes en la ficción, proviene del termino checo —robota— que significa “servidumbre” y tiene su origen en la comedia del escritor checo Karek Capek titulada *Los Robot Universales de Rossum* para designar a unas máquinas con aspecto humano que trabajaban en una fabrica.

En general se llama robot a aquellas máquinas que sustituyen al hombre u otro ser vivo en ciertas tareas, que por su peligrosidad o monotonía, u otros motivos, hacen mas recomendable o rentable el empleo de estas.

Los robots, normalmente incorporan alguna característica de los seres vivos, en forma de brazos, capacidad de movimiento, visión o tacto, que los diferencian de los automatismos, como pudiese ser un semáforo.

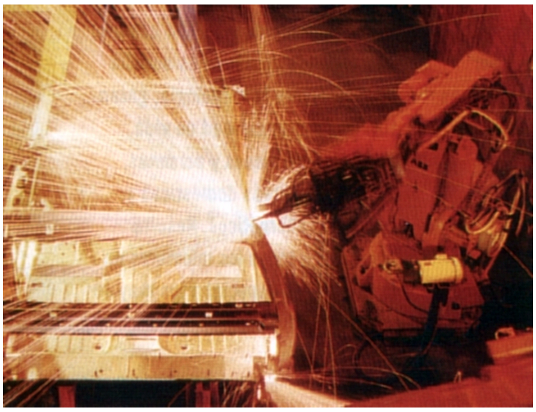

Figura 1.1: Una de las aplicaciones principales de los robots es en la industria de fabricación en serie.

Aunque en la ciencia ficción los robots suelen tener forma humana, en la practica, su aspecto es completamente diferente y viene determinado por las necesidades de utilización.

1.3. Microbots

A lo largo de los años, los robots han ido cambiando en sus características, los primeros robots eran mecanismos simples de gran tamaño que debían ser guiados para la realización de un determinado trabajo.

Con la llegada del microchip y los avances en las diferentes técnicas que engloba la robótica (automática, mecánica, electrónica, informática. . .) su tamaño se ha ido reduciendo, y su capacidad de funcionar si un guia humano aumentando, desde la capacidad de reproducir un movimiento repetidamente, hasta la de decisión en determinadas circunstancias, gracias a los avances en campos como las redes neuronales y sistemas expertos.

Los *Microbots* constituyen la parte de los robots de menor tamaño, en especial gracias a la aparición de los Microcontroladores, entre sus características destacarían:

- Pequeño tamaño.

Figura 1.2: MARV mide solo 12 mm. de altura.

- Incorporan medio de locomoción.
- Controlados por un chip microcontrolador.
- Económicos (versátiles y en ocasiones construidos con materiales reciclados).
- Carácter didáctico.

Aunque no siempre es así, en el libro Robots Móviles, Estudio y Construcción [1] se describen varios microbots, y ninguno incorpora un microcontrolador, Dyson y Electrolux han puesto en el mercado una aspiradoras, que son en realidad microbots, y ni Tienen carácter didáctico, ni son económicos, por citar un par de ejemplos.

Figura 1.3: Un ejemplo comercial de los microbots, aspiradoras.

Capítulo 2
Plataforma

La plataforma es la estructura mecánica que soporta todos los elementos que formar en Microbot.

En el caso de los microrobots, por sus características, bajo precio, alta disponibilidad en los materiales, fácil mecanización, la no necesidad de soportar grandes esfuerzos, hace que se suelan utilizar todo tipo de estructuras, desde placas de madera o metacrilato hasta cajas de galletas.

2.1. Plataforma de Piezas Comerciales

Figura 2.1: Microbot echo con piezas de mecano.

Una de las soluciones consiste en crear la plataforma a partir de piezas de construcción, habitualmente suelen utilizarse piezas de Mecano, o de Lego, dentro de la gama tecnic, proporcionan una gran versatilidad, gran resistencia mecánica, son económicas, y existen un conjunto de engranajes y partes móviles que facilitan la construcción del resto del robot.

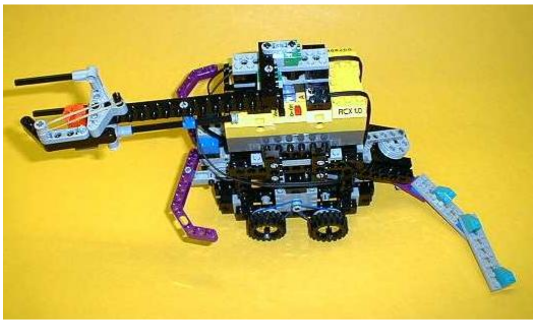

Figura 2.2: Microbot echo con piezas de lego.

2.2. Plataforma Comercial

Otra de las soluciones consiste en utilizar plataformas creadas por empresas específicamente para su uso en microbots, existen marcas como fishertechnik o cebek, que tienen un amplio catalogo de plataformas.

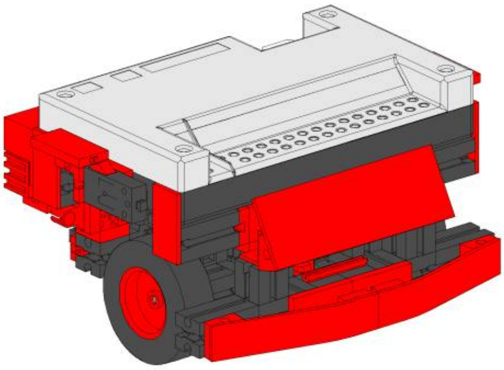

Figura 2.3: Estructura comercial de Fischertechnik.

Editoriales a través de colecciones y libros también tiene varios modelos de plataformas para microbots, en ocasiones incluyen además de la plataforma, los motores, servos o circuitos impresos necesarios para la fabricación del robot.

2.3. Plataforma Echa a Medida

Por ultimo en ocasiones resulta mas recomendable la construcción de la plataforma que se ajuste a las necesidades especificas del microbot.

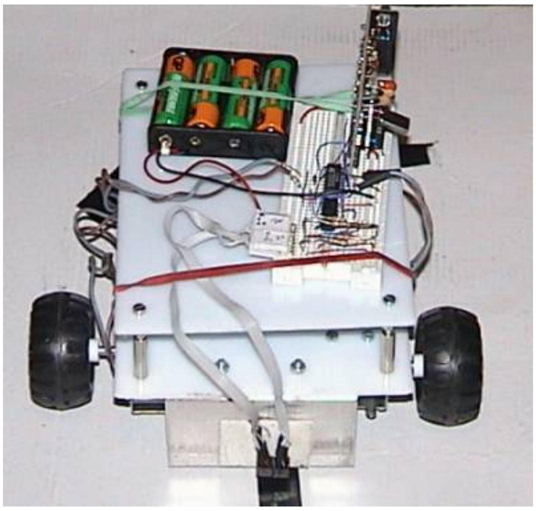

Figura 2.4: Trasto, la plataforma es una plancha de teflon.

Entre los materiales que se suelen utilizar esta la madera, el metacrilato, y laminas de hierro y aluminio de poco espesor, pues permiten un fácil manejo o mecanización, para adaptarlo a las necesidades especificas de cada robot.

2.4. El Microbot

La plataforma del Microbot esta dividida en dos partes:

Por un lado tenemos una plataforma comercial, sobre la que ira el circuito impreso principal, motores y baterías, utilizaremos la diseñada para el robot Cybot de Eaglemont Publications Ldt. ya que incorpora dos motores eléctricos con desmultiplicadoras y ruedas, ANSI como una rueda loca y soporte para las baterías, y diversas roscas donde sujetar soportes y placas de circuito impreso,con una calidad y resistencia mecánica aceptables y a bajo precio.

Esta plataforma es la versión comercial de un microbot llamado ”enanito”de la universidad de Reading.

La segunda plataforma sostiene los cuatro sensores de ultrasonidos, y sera de

Figura 2.5: Cybot, microbot del que aprovechamos la plataforma.

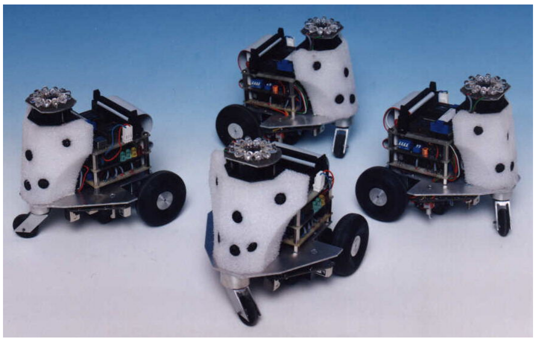

Figura 2.6: Los Enanitos, a partir de los que se creo Cybot.

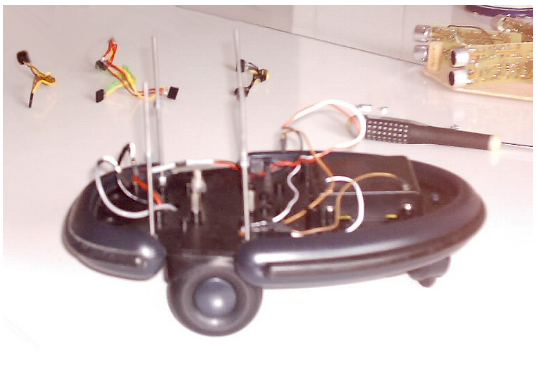

Figura 2.7: Plataforma del robot con las varillas roscadas y separadores para el circuito impreso.

construcción propia, en madera, y esta sujeta a la anterior por medio de varilla roscada de Métrica 3 y diversas tuercas.

Con esta plataforma mixta conseguimos por un lado un acceso fácil a la zona del microcontrolador, y la separación en módulos de las diferentes partes del robot, lo que supone una facilidad a la hora de comprobar el funcionamiento de cada parte y una colocación de los sensores adecuada a las necesidades de nuestro robot.

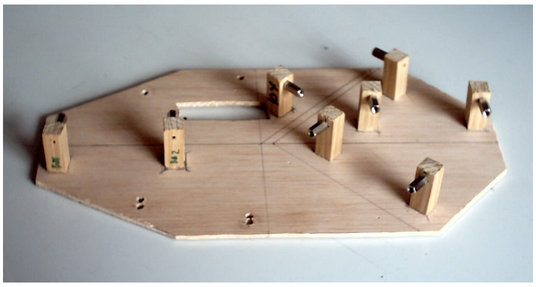

Figura 2.8: Plataforma que soportara los sensores.

Además crearemos una pieza en hierro, que se atornillara a la plataforma comercial y que contendrá una de las baterías.

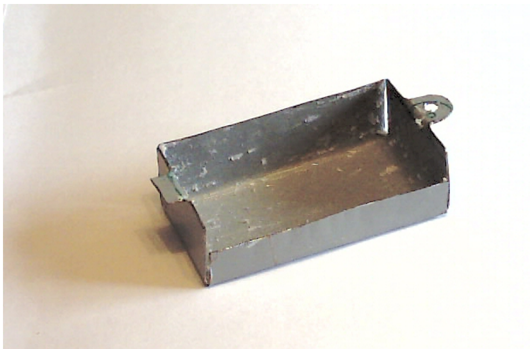

Figura 2.9: Portapilas.

Capítulo 3

Sistema de Locomoción

Una de las características de los Microbots es que son capaces de moverse, para realizar este cometido existen diferentes opciones:

3.1. Patas

En muchas ocasiones los robots intentan ser imitación de la naturaleza, de hay que el uso de patas en robots, se considere desde cierto punto de vista lógico.

En los robots, existe el problema principal del equilibrio:

Un robot se mantiene en equilibrio estático cuando su centro de gravedad esta situado en el interior de la superficie delimitada por los puntos de apoyo del robot, y no existen fuerzas que lo muevan.

Cuando el centro de gravedad esta fuera de esa superficie, genera unos momentos de fuerza que tienen a hacer desplazarse al robot, un robot se encuentra en equilibrio dinámico cuando genera unos momentos contrarios a estos, que evitan que el centro de gravedad se desplace, y el robot pierda el equilibrio.

Hasta hace poco tiempo los sistemas no eran lo suficientemente avanzados para permitir que un robot con solo dos patas (en equilibrio dinámico, puesto que la superficie entre los puntos de apoyo es una linea, y su centro de gravedad no cae nunca dentro de esa linea) se mantuviese en pie, y puesto que la tecnología que consigue esto es complicada y precisa normalmente de gran cantidad de cálculos y alta precisión en los movimientos, se utilizan un numero superior de patas que evita este problema.

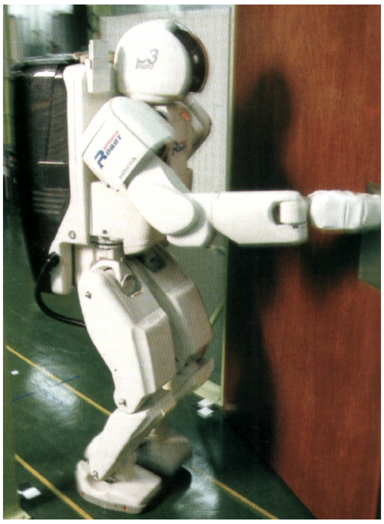

Figura 3.1: el P3 de Honda es el fruto de 10 años de investigación.

3.1.1. Cuatro Patas

A partir de 4 patas es posible mantener equilibrio estático, aunque una de ellas no estuviese tocando el suelo, lo que permite el movimiento del aparato, moviendo una pata cada vez, sin necesidad de preocuparse por la perdida del equilibrio.

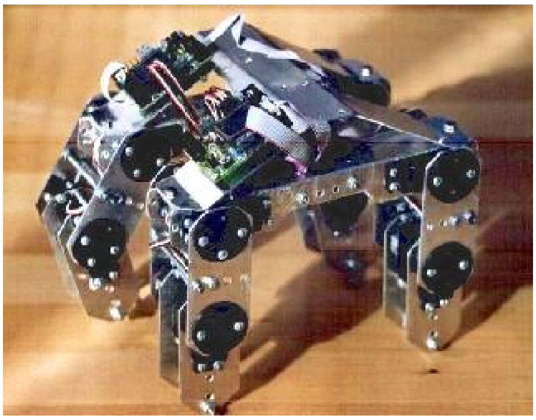

Figura 3.2: Pucho, un microbot de cuatro patas.

Tiene la ventaja de que es posible calcular la posición del robot sin necesidad de referencias externas o sensores.

Como desventaja su movimiento lento, al solo poder levantar del suelo una pata de cada vez.

3.1.2. Seis o mas Patas

Con 6 patas es posible mantener hasta 3 patas sin tocar el suelo, esto permite una mayor rapidez de movimientos, en contra es mas fácil que se produzcan desplazamientos en los giros, lo que impide un calculo preciso de su posición.

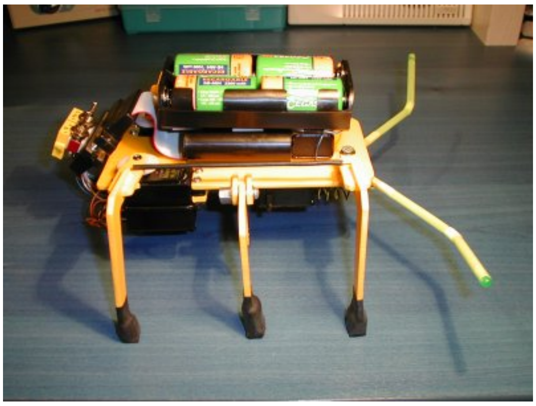

Figura 3.3: Microbot de seis patas.

En ocasiones estas patas son solidarias 2 a 2, y de movimientos limitados, hacia adelante y atrás, o arriba y abajo únicamente, permitiendo reducir el numero de motores necesarios.

3.2. Orugas

Las orugas permiten mayor agarre que cualquier otro método, pues la superficie de contacto es mucho mayor, permiten además sortear pequeños obstáculos, y no requieren de suspensión, pues siempre hay al menos una sección de cada oruga tocando el suelo.

En contra, al igual que con las seis patas, se pueden producir desplazamientos en los giros, lo que impide un calculo exacto de su posición.

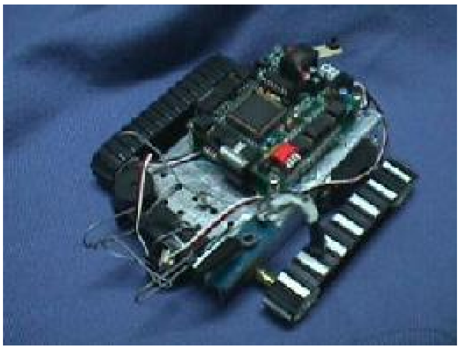

Figura 3.4: Vigilante, Microbot con orugas

3.3. Ruedas

Las ruedas es probablemente el método mas sencillo de implementar a la hora de dotar a un robot de un medio de desplazarse, ya que la complejidad mecánica necesaria es mucho menor que en las opciones anteriores.

3.3.1. Amortiguación

La amortiguación cumple la función de absorber las irregularidades del terreno, permitiendo que las ruedas siempre toquen el suelo, y evitando que el cuerpo del robot vibre con las irregularidades del terreno.

Se utilizan dos sistemas, una basado en muelles y amortiguadores, y otro basada en la flexibilidad del material con el que se hacen las ruedas, la necesidad de uno o ambos vendrá determinado por el terreno en el que se use el robot.

3.3.2. Numero de Ruedas

por razones similares a las explicadas con las patas, es necesario que al menos el microbot disponga de tres ruedas.

Un mayor numero de ruedas implica una superficie de apoyo mayor lo que permite mejorar el equilibrio del robot, pero a partir de cuatro ruedas es necesario que el robot este dotado de amortiguación, pues es posible que las irregularidades del terreno dejen alguna de las ruedas en el aire, si la rueda que queda en el aire es una de las tractoras, el movimiento del robot o se anulara, o no sera el esperado.

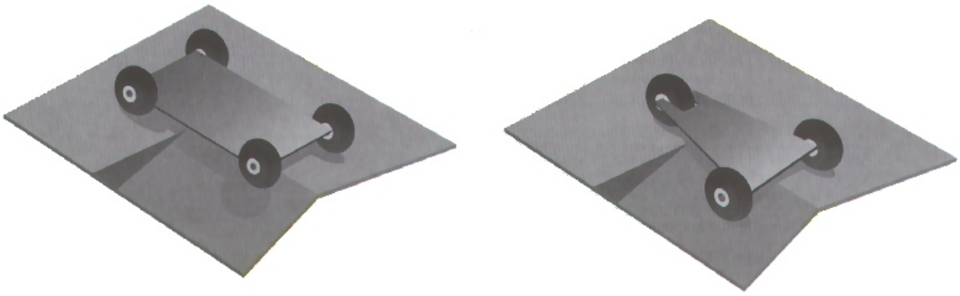

Figura 3.5: Ante irregularidades del terreno, con 3 ruedas no hace falta suspensión

Figura 3.6: Robot de 10 ruedas para mejorar la estabilidad

3.3.3. Ruedas Directoras

Es el sistema actualmente utilizado en los coches y motos, unas ruedas giran sobre su eje Z para dirigir el vehículo lateralmente, mientras que otras ruedas (pueden ser las mismas) que giran en el mismo sentido para mover el vehículo frontalmente.

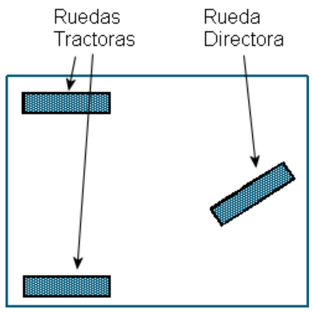

Figura 3.7: Configuración de ruedas Directoras.

Su principal ventaja esta en que solo necesita un motor que desarrolle la potencia para mover el vehículo.

En su contra que no es posible girar sobre su propio eje, lo que dificulta el movimiento o posición en determinadas circunstancias, p.e. en zonas estrechas.

En caso de que existan varias ruedas tractoras y estas sean solidarias, y en función del peso, tamaño y velocidad que alcance el robot, puede ser necesario que incorpore un sistema de tracción diferencial, ya que en las curvas, las ruedas giran a diferente velocidad, y de no incorporar este sistema las ruedas derraparían.

3.3.4. Ruedas Diferenciales

Con esta configuración, un numero de ruedas par, con motor independiente, permiten al vehículo girar sobre su propio eje Z. Variando la velocidad de una de las ruedas con respecto a la otra es posible realizar giros de diferente radio.

En esta configuración, la otra rueda necesaria suele denominarse loca, y es de giro libre sobre su eje Z.

Permite una mayor libertad de movimientos, y simplifican los cálculos de posición del robot sin referencias externas.

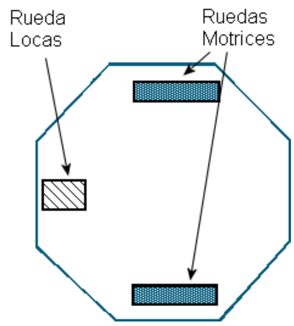

Figura 3.8: Configuración de ruedas Diferenciales.

3.3.5. Giro Sincronizado

En esta configuración todas las ruedas además de permitir el desplazamiento del robot, tienen un giro en el eje Z de 360º.

Esto permite al robot en moverse en cualquier dirección sin cambiar su orientación, lo que lo hace especialmente útil en zonas con muchos obstáculos.

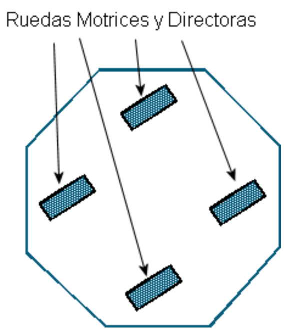

Figura 3.9: Configuración de Giro Sincronizado.

Por contra su complejidad mecánica es muy elevada.

3.4. El Microbot

El microbot utilizara tres ruedas, en configuración de ruedas diferenciales

La amortiguación estará basada únicamente en la flexibilidad de las ruedas echas de caucho.

Dos ruedas serán motrices, cada una equipada con un juego de engranajes desmultiplicadores para aumentar su potencia.

La tercera rueda, mas pequeña, y situada en la parte delantera sera de giro libre, utilizándose únicamente para dar estabilidad al conjunto.

Esta rueda tiene el eje de giro retrasado con respecto al eje Z, lo que hace que se oriente sola en la dirección de movimiento del robot.

Capítulo 4

Motorización

Tanto en el caso de usar patas, como ruedas o orugas, como en el caso de disponer de brazos, u otro elemento móvil, es necesario disponer de un sistema que realice este movimiento.

4.1. Alambres Musculares

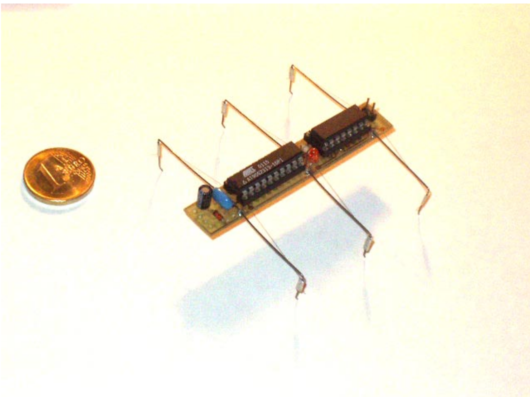

Figura 4.1: Stiquito, sus patas se mueven con hilos de flexinol.

Están basados en la propiedad de dilatación de los cuerpos con la temperatura y en el calentamiento de los mismos al pasar una corriente a su través.

Uno de los mas utilizados son los "Muscle Wires" de la empresa Mondo Tronics, compuestos por una aleación llamada Nitinol de Níquel y Titanio desarrollados por el U.S. Naval Ordnance Laboratory (de hay su nombre Ni-Ti-N-O-L) mientras buscaba una aleaccion resistente a la corrosión, aunque este efecto ya había sido observado en 1932 por el investigador suizo Arne Ölander en aleaciones de oro y cadmio, se les llama aleaciones con memoria de forma, y tienen múltiples aplicaciones comerciales.

El Nitinol se comercializa con la marca flexinol, en diferentes diámetros y temperaturas de trabajo (entre 70º y 90º), pueden variar su longitud hasta un 8 %-10 % aunque se recomienda no exceder el 5 % para evitar fatiga del material.

Al circular una corriente se calientan y encogen, volviendo a su forma original al enfriarse, este proceso es lento y puede llevar varios segundos en función de la temperatura ambiente y forma del alambre.

Son ligeros, de alto rendimiento eléctrico, muy poco espacio (pueden utilizarse donde no cabe ningún tipo de motor), y son silencioso.

En su contra son caros, y lentos y no es posible soldarlos.

4.2. Actuadores Hidráulicos

Normalmente de uso exclusivo en robots con patas o en brazos, una serie de cilindros y tubos permite mediante el desplazamiento de un fluido (aire o aceite) el movimiento.

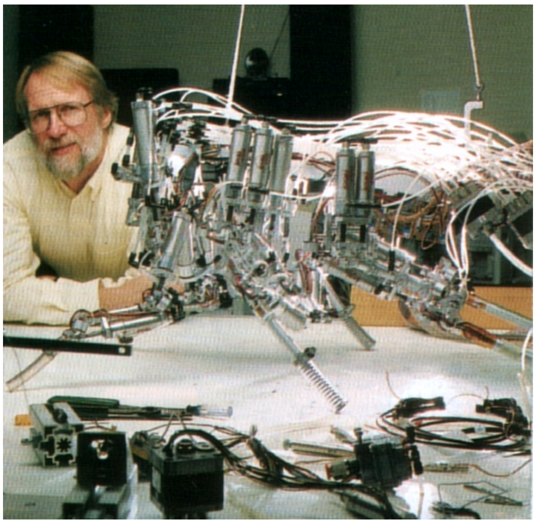

Figura 4.2: Los Actuadores hidráulicos complican la mecánica del robot.

Tienen un gran resistencia a los sobreesfuerzos, y pueden ser muy silenciosos, pero necesitan de un sistema que genere presión, y tienen una gran complejidad de tubos lo que los hace muy voluminosos y delicados.

4.3. Motores Neumático o Hidráulico

Una de las ventajas de los motores neumáticos o hidráulicos en robots, es que son capaces de desarrollar su máxima potencia a cualquier velocidad de giro, tienen poca inercia y gran capacidad de aceleración, además de soportar sin problemas sobrecargas.

Igual que los sistemas de cilindros, tienen el inconveniente de la complejidad de tubos necesaria y el sistema que genere presión.

4.4. Motores Térmicos

Útiles en vehículos que requieran gran potencia, solo son útiles en ciertos microrobots, donde sea necesaria una gran potencia o velocidad de desplazamiento, tienen el gran inconveniente de necesitar de sistemas de arranque, embrague y cambio de sentido de giro o marchas, requieren además un control constante de los parámetros de funcionamiento, además de que generan gran cantidad de gases durante su funcionamiento.

Existen un amplio catalogo de motores de 2 tiempo y de cuatro tiempos de cilindradas pequeñas, gracias a su amplio uso en modelismo radiocontrolado.

4.5. Motores Paso a Paso

Existen principalmente dos tipos de motores eléctricos, los de giro continuo, analizados mas adelante, y los motores paso a paso.

Estos motores incorporan un cierto numero de bobinas en el estator y un imán permanente en el rotor, están diseñados para girar un numero determinado de grados en una dirección cuando se les aplica tensión.

Mediante la actuación en las diversas bobinas, es posible controlar la cantidad de grados que gira y el sentido, el paso suele estar estandarizado en un divisor de la circunferencia, p.e. en 1,8º (Una vuelta completa son 200 pasos), en función de las bobinas podemos clasificarlos en tres categorías:

Figura 4.3: Un motor paso a paso.

Motores Bipolares. Incorporan dos bobinas, por las que puede circular corriente en ambos sentidos, externamente se suelen identificar por tener cuatro cables, la electrónica necesaria para controlarlos es mas complicada por la necesidad de circular la corriente en ambos sentidos.

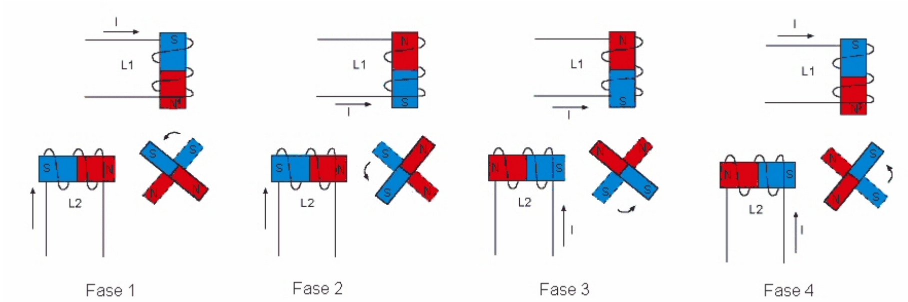

Figura 4.4: Secuencia de energizacion en un M.P.P. bipolar.

Motores Unipolares Incorporan dos pares de bobinas, normalmente con uno de los bornes de cada par unidos, las corriente circula por las bobinas siempre en el mismo sentido y de identifican externamente por tener cinco o seis cables, suelen ser de un tamaño ligeramente superior a los bipolares.

Motores Multifase Incorporan múltiples bobinas, bipolares conectadas en serie, en cada momento, todas las bobinas menos una están activadas, lo que le da un gran par de movimiento.

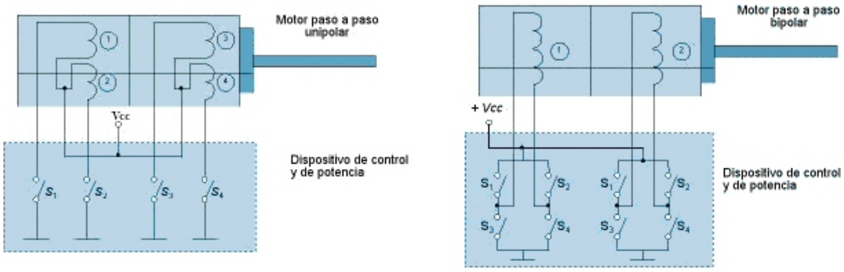

Figura 4.5: Conexión eléctrica de dos tipos de Motores paso a paso.

Mediante el interfaz adecuada es posible controlar la posición del eje, su velocidad y sentido de giro.

Son capaces además de desarrollar un gran par motor, por contra suelen tener un coste mas elevado.

4.6. Servos de Modelismo

Un servomotor es un conjunto de un motor eléctrico, y un circuito realimentado en bucle cerrado, que permite ajustar con precisión el movimiento o velocidad del motor sin necesidad de utilizar un motor paso a paso.

Figura 4.6: Servos de modelismo.

Los servos de modelismo, incluyen en una caja de reducido tamaño, un motor eléctrico, un grupo de engranajes, y circuito de control eléctrico en bucle cerrado, en un encapsulado estándar, y a unos precios muy reducidos y una amplia gama de pares motores, gracias a su amplia utilización en modelismo radiocontrolado.

El grupo de engranajes le confiere un gran par motor, lo que lo hace muy útil en robots para el manejo director de brazos, patas o ruedas directoras.

Mediante una única señal pulsante modulada en amplitud es posible controlar la posición exacta del eje, esto lo hace especialmente útil en microrobotica, pues reduce la electrónica necesaria y maximiza el numero de actuadores por microcontrolador.

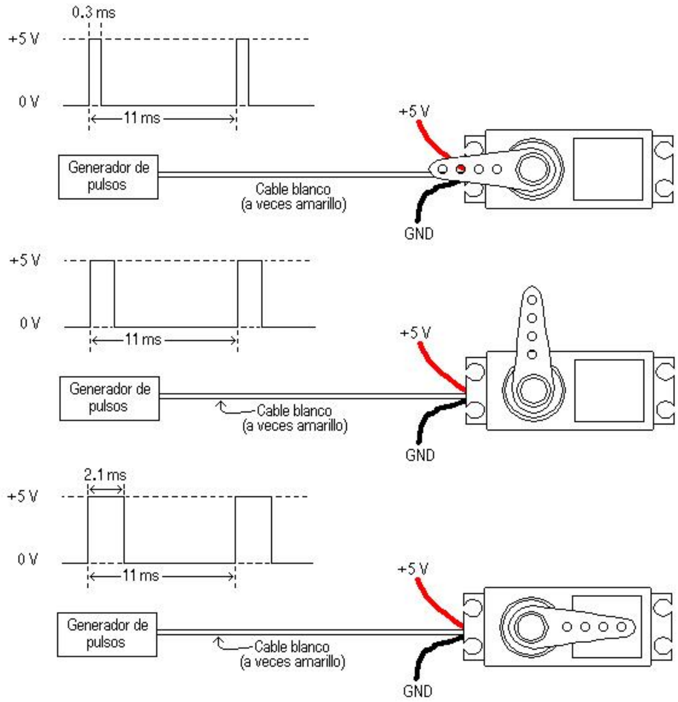

Figura 4.7: Control del servo mediante pulsos.

Con unas pequeñas modificaciones consistentes en la sustitución de un potenciómetro y la eliminación de una muesca en el juego de engranajes es posible mediante la misma señal del pulsos controlar el giro sin fin del eje en cualquier dirección y en cualquier velocidad, adecuado para ruedas tractoras.

El control se realiza variando el ancho del pulso, sin importar (dentro de unos margenes) su frecuencia, con una señal TTL, esto lo hace muy útil para su manejo con microcontroladores, pues solo utiliza una linea de I/O y la programación es muy sencilla, llegando en el caso de utilizar lenguajes de alto nivel a existir ordenes especificas para su manejo.

Como inconvenientes destaca la salida del eje de los engranajes que puede no ser lo mas adecuado para ciertas aplicaciones.

4.7. Motores Eléctricos

Existe un amplio abanico de motores eléctricos, tanto de corriente alterna como de corriente continua, de todo tipo de potencias y tensiones, nos centraremos en los motores de corriente continua (DC) de baja tensión.

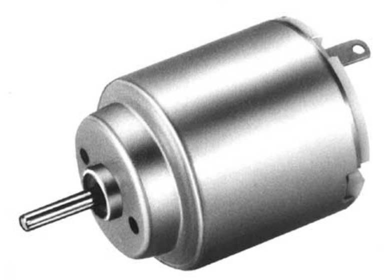

Figura 4.8: Típico motor DC.

Su sentido de giro viene determinado por la polaridad de alimentación, y su velocidad por la tensión aplicada (influyen otros parámetros, como la carga que soporta por ejemplo).

Son baratos y de fácil adquisición en cualquier tamaño o potencia.

Están compuestos por un eje de acero sobre el que se coloca el rotor y el colector.

El rotor, formado por un núcleo de laminas de hierro sobre el que están varias bobinas, de hilo de cobre esmaltado, conectadas eléctricamente al colector, el núcleo de hierro reduce las perdidas parasitarias y por histeresis de las bobinas.

El colector formado por unas laminas de cobre, llamadas delgas cumple la función de proporcionar la corriente en el momento y sentido adecuado.

Una carcasa sobre la que esta situado el estator, formado por un imán permanente, y unas escobillas formadas por un material mas blando que el colector (para evitar su desgaste) y que proporcionan la corriente desde el exterior.

4.8. Manejo de Motores Eléctricos

Los microcontroladores no son capaces de proporcionar la intensidad que necesita un motor para su funcionamiento, además estos, debido al uso de bobinas, generan gran cantidad de ruidos electromagnéticos he interferencias que afectan y llegan a destruir los microcontroladores y otros componentes electrónicos, se hace necesario entonces el uso de un circuito de control de los motores, llamado “driver” que haga de intermediario.

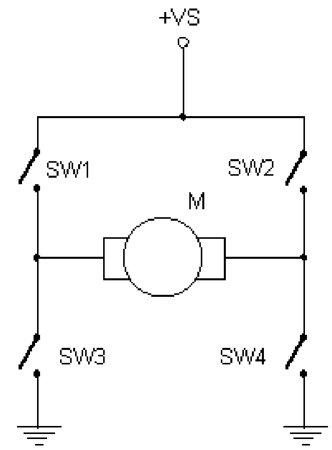

Figura 4.9: Esquema de un puente en H.

Este driver es además necesario en los casos en que hay que invertir la polaridad en las bobinas, o si se trabaja con fuentes simétricas.

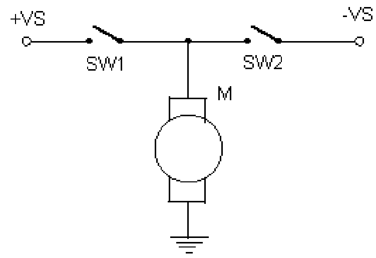

Figura 4.10: Esquema con alimentación doble.

Suelen incorporar además un sistema de condensadores y diodos, cuya misión es filtrar la corrientes generadas por las bobinas y los parásitos que de otra maneja quemarían los componentes semiconductores del circuito.

En la mayoría de los casos se requiere que la corriente circule en ambos sentidos por el motor, p.e. para controlar el sentido de giro, una de las soluciones es utilizar un sistema de alimentación simétrica, esto reduce el numero de interruptores, y la potencia perdida en ellos, pero requiere un volumen doble para el sistema de energía (las baterías).

Otro de los sistemas que se utiliza para controlarlos son los puentes en H, tienen la ventaja de que no necesitan alimentación simétrica, están compuestos por cuatro interruptores que activados dos a dos, permiten que la corriente circule en ambos sentidos por el motor, mientras que por los interruptores siempre circula por con en el mismo sentido, facilitando la protección del interruptor mediante diodos.

Estos interruptores pueden ser:

Control por Reles

Este sistema tiene las ventajas de que la caída de tensión, y la disipación de potencia son nulas, permitiendo grandes potencias.

Como inconveniente, su ruido, la imposibilidad de conmutaciones rápidas, y por ello no se puede utilizar la velocidad por PWM, y la necesidad de un circuito adicional para poder ser controlado por el microprocesador, puesto que los relés tienen los mismos inconvenientes que los motores.

Transistores

Las ventajas de los transistores, es su bajo coste. La desventaja, las perdidas que se producen, no haciéndolo muy adecuado para grandes potencias.

Mosfet

Los mosfet, tienen una caída de tensión mas baja, permitiendo su uso en grandes potencias, por contra, necesitan una tensión alta, no haciéndolos adecuados para pequeños robots que funcionan con 12V o menos.

Circuitos Integrados

Existen varios circuitos que pueden ser utilizados para sustituir a los transistores y mosfet, permitiendo, una baja tensión de uso, pocas perdidas, posibilidad de controlar la tensión por PWM y control directo desde el microprocesador, en ocasiones traen sistemas de protección contra sobrecarga.

4.9. El Microbot

El microbot utilizara dos motores de corriente continua de Mabuchi modelo RE-140RA de 6V, he incorporan 2 condensadores para eliminar parásitos producidos en el arranque y parada.

El control sobre el sentido de giro del motor se realiza mediante el integrado L293D en configuración de puente en H, que además aisla la parte de potencia de la parte lógica he incorpora protección contra sobrecargas.

Se ha utilizado el montaje que recomienda el fabricante del chip de control en la Nota de Aplicación [7], con cuatro diodos por bobina, para absorber las corrientes que generan las bobinas.

Capítulo 5

Sistema de Energía

Tanto en el caso de los circuitos eléctricos o electrónicos de control, como en el caso de motores, servos u otros aparatos eléctricos que produzcan movimientos, es necesario una fuente de energía.

En el caso de energía eléctrica, la capacidad de los dispositivo se mide en Amperios en una Hora, y nos permiten determinar cuanto tiempo va a poder funcionar el robot.

Veremos ahora las opciones que permiten crear un sistema autónomo.

5.1. Células Solares

Las células solares proporcionan muy poca potencia en relación al espacio que ocupan y tienen un coste muy alto, además suele ser necesario una batería o pila recargable, que permita almacenar la energía para momentos en que se necesite mas potencia de la que puede generar, p.e. al colocar la célula en una zona de sombra.

Su utilización solo esta justificada en aquellos casos en que sea necesario que el robot funcione indefinidamente sin intervención humana, y solo como elemento complementario.

5.2. Pilas y Baterías

Las pilas y baterías están basados en la capacidad que tienen dos materiales, llamados cátodo y ánodo, de producir electricidad cuando se ponen en contacto por medio de un tercer material llamado electrólito, por medio de una reacción química en la que se transforma el electrólito.

Figura 5.1: Robot en otros planetas es un ejemplo de donde si esta justificado el uso de células solares

En función de estos materiales diferenciamos varios tipos:

5.3. Baterías de Plomo

Las baterías, tienen la ventaja de ser recargables, teniendo normalmente un electrodo de plomo, del que reciben el nombre, tanto en el caso de las baterías con mantenimiento, tipo automóvil, como las que van selladas, requieren de electrónica adicional para su carga, y suelen ser de gran tamaño y peso.

El elemento electrólito de las baterías de plomo suele ser una disolución de ácido sulfúrico, con las necesidades de tomar medidas de precaución que ello conlleva.

5.4. Pilas Secas

Se denominan así, por que a diferencia de las baterías de plomo el electrólito no es liquido, se suelen llamar también salinas o alcalinas, en función del compuesto del electrólito (del que depende su capacidad) están disponibles en varias gamas de capacidades para una misma dimensión, pero de un solo uso, proporcionan 1,5V por elemento, tensión que decae a medida que se gasta.

Figura 5.2: Diferentes Encapsulados de Pilas

5.5. Pilas Recargables

Existen varios tipos, cada una de ellas con mas capacidad que la anterior, proporcionan 1,2V por elemento, y una resistencia interna mucho mas pequeña lo que hace que su tensión decaiga mucho menos a medida que se gastan.

Los tipos de pila tienen la ventaja de que existen en el mercado en unos formatos estándar, lo que permite su intercambio si los valores de tensión no son un problema.

5.5.1. Níquel-Cadmio

las pilas de Ni-Cd requieren de un mantenimiento especial, pues solo deben ser recargadas cuando esta casi agotadas, para evitar el efecto de memoria.

5.5.2. Iones de Litio

Las pilas de Iones de Litios, tiene una tensión por celda mayor, en torno a los 2V, son las que mas capacidad dan, no soportan las sobrecargas, y requieren de una electrónica especial para su carga, que se puede hacer en cualquier momento.

5.5.3. Níquel Metal-Hidruro

Las pilas de Ni-Mh proporcionan un equilibrio, con una capacidad intermedia, sin efecto memoria y posibilidad de carga en cualquier momento, y tienen capacidad para soportar sobrecargas lo que permite que el circuito de carga sea tan sencillo como una resistencia entre ella y la fuente de tensión.

5.6. Sección de Potencia

Los motores y actuadores eléctricos del robot, tienen unas necesidades diferentes a la parte lógica.

No suelen ser sensibles a los cambios de voltaje, suelen necesitar un mayor amperaje, y tener picos de tensión debido a las cargas inductivas de los motores.

Se suele utilizar una alimentación separada de la lógica, y se pone especial cuidado en aislar ambas partes, por medio de reles, optoacopladores o circuitos integrados especiales, además de colocar filtros con condensadores en diversas partes del circuito para reducir posibles picos e interferencias.

5.7. Sección Lógica

La parte lógica del robot, suele estar formada por circuitos integrados, que requieren una alimentación estable, y el el caso de los C.I. TTL precisa de 5V, por lo que se hace necesario un sistema que asegure esos valores.

En función de las necesidades de corriente del dispositivo se pueden utilizar varios sistemas de estabilización.

La estabilización por medio de componentes discretos, p.e. diodos zener, adolece de ciertas limitaciones, que lo hacen poco recomendable para este tipo de circuitos.

Existen circuitos integrados capaces de proporcionar una tensión estabilizada a un rango de intensidades mayor, como la serie LM78XX y el LM317, que requieren muy pocos componentes externos.

5.8. El Microbot

La energía para el robot viene proporcionada por dos grupos de pilas.

La parte de potencia se alimenta por cuatro elementos de tipo AA, que en el caso de las pilas de Ni-MH proporcionan 4,8-6V y 1500mA, lo que proporciona una gran autonomía.

La parte Lógica se alimenta con un elemento tipo 6F22, de 9V y 150mA, y es estabilizada por un integrado LM7805, proporcionando los 5V que necesita el microcontrolador y el resto de circuitos integrados, con una intensidad máxima de 1.5A.

La tensión de la parte lógica también se utiliza para los sensores de ultrasonidos, ya que como no incorporan elementos inductivos no interfieren con el resto del circuito.

Capítulo 6

Sensores

Para que el robot pueda interactuar con el mundo exterior, necesita de una serie de sensores, que transformen las diferentes magnitudes a niveles de tensión, o valores binarios, que el sistema de control utilizara para decidir que hacer.

Estos sensores son también utilizados para obtener realimentación del funcionamiento de partes del robot, p.e. para comprobar que dos ruedas que deben girar a la vez, lo hagan y no una mas rápida que otra.

6.1. Sensores de Contacto o Mecánicos

Los sensores de contacto, se utilizan sobretodo en parachoques, y para determinar cuando se ha llegado al limite de movimiento de una pata o brazo, una estructura activa un interruptor que permite determinar su posición.

Figura 6.1: Microinterruptores utilizados en sensores de contacto.

6.2. Sensores de Posición

Normalmente construidos con potenciómetros, y conectados a un conversor analógico-digital (DAC) permiten saber la posición exacta te un brazo o pata.

En ocasiones no es necesario el conversor analógico digital, utilizando en su lugar una red RC y sabiendo el valor del condensador, se calcula el valor de la resistencia por software.

6.3. Luz Visible

Suelen estar basados en una LDR o fototransistor, y permiten distinguir luces y sobras, p.e. para que el robot siga una linterna, o busque al sol.

Figura 6.2: Las LDR(Resistencias Dependientes de la Luz) se utilizan como sensores.

También es posible utilizarlos para seguir lineas dibujadas en el suelo, o controlar el movimiento de una estructura, pero tienen el inconveniente de que son muy sensibles a cambios de luz e interferencias exteriores.

6.4. Luz Infrarroja

Similares a los sensores de luz visible, son menos sensibles a las interferencias externas, permitiendo una mayor precisión.

Existen conjuntos de sensores, en encapsulados especiales, con un emisor de luz infrarroja, normalmente un led, y un fotodiodo o fototransistor, colocados de manera que pueden ser utilizados directamente para el control de movimiento, o velocidad de giro, mediante discos ranurados (si los sensores están enfrentados), o dibujos sobre una superficie (si los sensores van paralelos).

Si se utilizan discos ranurados, se les denomina sensores relativos, pues solo permiten determinar (sin una referencia) la cantidad de movimiento. Colocando varios sensores desplazados sobre la superficie es posible saber el sentido en que se desplaza.

Si lo que interesa es conocer su posición, se utilizan varios sensores (el numero de sensores es igual a la resolución en bits) sobre una superficie en la que hay un dibujo basado en el sistema binario Gray. El código binario Gray se diferencia del tradicional en que solo cambia un bit de valor de cada vez, lo que permite aumentar la fiabilidad de estos sensores, a este tipo de sensores se les denomina absoluto, pues permiten determinar la posición del elemento que tiene el sensor.

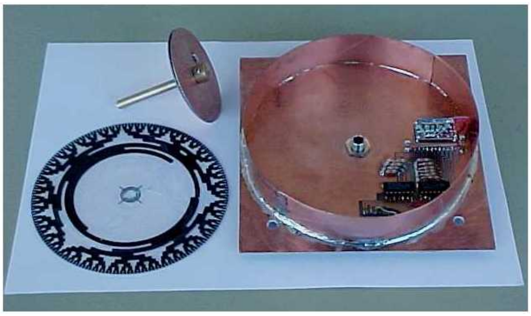

Figura 6.3: Sensor Rotatorio Absoluto, nótese el dibujo en código Gray del disco.

También es posible utilizarlos en medida de distancias, midiendo el ángulo con el que la luz es reflejada y vuelve al sensor, por triangulación es posible calcular la distancia, tiene la ventaja de que la medida es instantánea, y la desventaja de que depende del color y textura del objeto para poder dar una medida precisa, y tener un rango de medida limitado.

Normalmente este tipo de sensores vienen en un encapsulado especial que incorpora el emisor, el receptor y la lógica necesaria para obtener la medida de distancia.

6.5. Sensores de Posición Absoluta

Bajo este epígrafe se engloban varios sensores que permiten al robot saber su posición con respecto del entorno sin una referencia fija.

Figura 6.4: el GP2D02 de Sharp mide distancias por infrarrojos.

Cápsulas de Mercurio, contienen dos contactos y mercurio en su interior, cuando el sensor se inclina unos grados determinados, el mercurio une los contactos.

Figura 6.5: Sensores de mercurio, permiten saber si el robot se inclino a un determinado ángulo.

Brújulas Electrónicas, que proporcionan una señal analógica o digital (según el modelo) que indica la orientación del sensor con respecto al norte de la tierra.

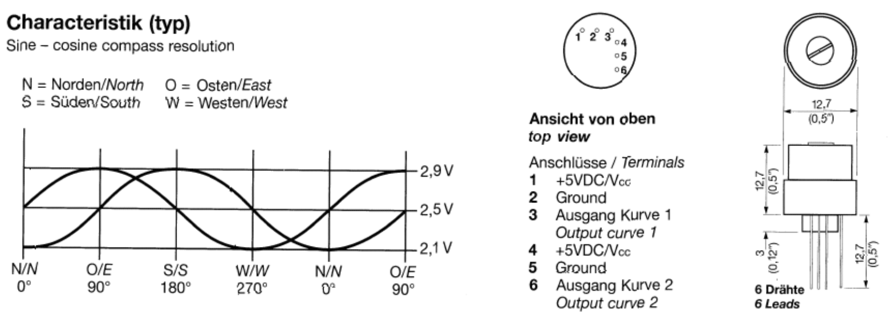

Figura 6.6: Características de una Brújula electrónica.

Acelerometros y giroscopios, similares a las brújulas electrónicas, proporcionan una señal que permite determinar si el sensor se ha desplazado, o rotado en una dirección.

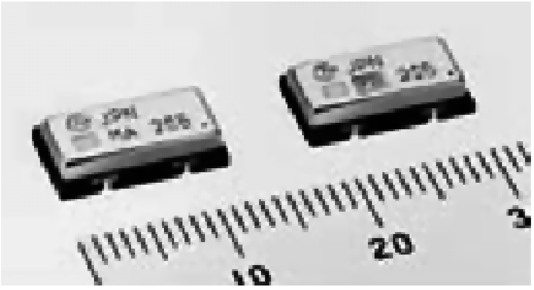

Figura 6.7: Giroscopio electrónico piezoeléctrico

6.6. Otros Sensores

Existen diversos integrados sensores de temperatura, desde encapsulados de 3 patillas, como el lm335, que proporcionan un valor analógico, hasta aquellos que proporcionan el valor en formato digital, con protocolo I2C como el LM75.

En aplicaciones especificas los microbots también pueden incorporar otros sensores, basados en diversas propiedades capacitivas, magnéticas (de efecto HALL) o inductivas, permiten determinar cuando un objeto pasa cerca de el, o incluso seguir lineas de tensión bajo suelos o paredes.

6.7. Ultrasonidos

Por ultimo, es posible utilizar sensores de ultrasonidos, que de una forma similar a como funcionan los murciélagos, permiten medir distancias o la presencia de objetos.

6.7.1. Los Ultrasonidos

Lo que conocemos por sonido es la sensación que se produce en nuestro oído, al existir un cambio en la presión del aire, que incide en los tímpanos.

El tipo de sonido depende de la forma, magnitud y frecuencia a la que este cambio de presión se produce, el oído humano es capaz de sentir sonidos cuya frecuencia oscile entre los 20Hz y 20.000Hz aproximadamente, algunos animales tiene el oído mas sensible y sus limites de frecuencia son mayores.

El rango de los ultrasonidos, esta fuera del alcance del oído humano y va desde los 20KHz hasta los 500KHz, normalmente en los sensores de ultrasonidos se emplea la frecuencia de 40KHz, una frecuencia baja para facilitar el diseño de los circuitos electrónicos, pero suficientemente alta como para no molestar a personas o animales domésticos.

La magnitud con la que se recibe el sonido se mide en decibelios, y es lo alto o bajo que escuchamos el sonido, la sensibilidad de los humanos varia con la frecuencia, y en general a partir de los 100dB, puede producir daños físicos en el oído.

La forma de la onda, es lo que solemos denominar timbre y nos permite distinguir entre dos sonidos.

Cualquier forma de onda no senoidal, puede ser descompuesta en una suma de una onda senoidal llamada fundamental, y de otras de frecuencias múltiplos de la fundamental, llamadas armónicos, de ahora en adelante cuando hablemos de sonido nos referiremos a una onda senoidal, y en caso de no ser así, su funcionamiento podría considerarse que es la suma de los funcionamientos de las señales que la componen.

Estos cambios de presión se propagan a través de diferentes medios en forma de ondas. la velocidad y atenuación en el tiempo de esta onda depende del medio por el que se propaga, y de las condiciones de presión, humedad y temperatura.

La frecuencia también influye en grado de dispersión de la onda, y a mayor frecuencia la señal es mas ”direccional”

6.7.2. Medidas Mediante Ultrasonidos

Si emitimos una serie de ultrasonidos, y estos chocan contra los obstáculos, devolviendo un eco hacia el lugar donde se emitió, midiendo el tiempo que tarda este en volver desde que se emitió el sonido, podemos calcular el espacio que ha recorrido, y la mitad sera la distancia que nos separa del obstáculo.

Podemos que en condiciones normales, el sonido viaja a $341\ ms^{-1}$, y así podemos calcular la distancia como:

$$d = \frac{vt}{2} = 170{,}5t \tag{6.1}$$

Siendo t el tiempo que pasa desde que se empieza a emitir el ultrasonido hasta que se recibe el eco.

Debido a la captación directa de los sonidos, y al espacio necesario para que la señal rebote, los ultrasonidos no se suelen utilizar para medidas inferiores a 10cm.

Debido a la dispersión y atenuación del sonido con la distancia, el limite superior de medida con ultrasonidos esta en torno a los 9 o 10m.

6.7.3. Transductores Piezoeléctricos

Son los elementos que emiten y captan los ultrasonidos, tienen un funcionamiento similar al micrófono y al altavoz, pero se basan en otro fenómeno físico, ya que estos no son capaces de trabajar en el rango de los ultrasonidos.

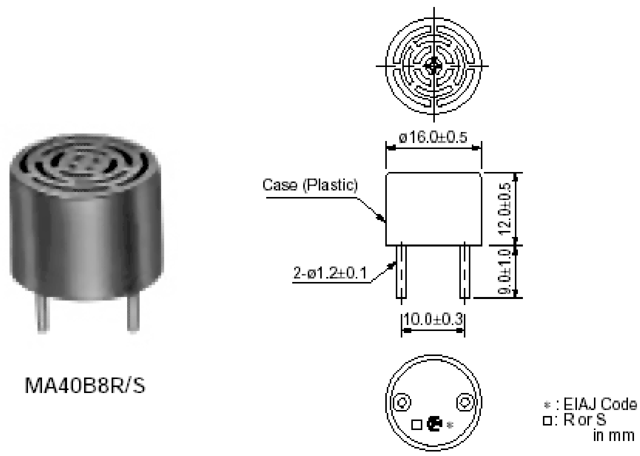

Figura 6.8: Características de un transductor de ultrasonidos.

Se basan en la capacidad de algunos cristales de vibrar cuando se les aplica energía, y producir energía cuando vibran, a esto se le denomina efecto piezoeléctrico.

Eléctricamente se comportan como un conjunto RCL mixto.

6.7.4. Descripción del Funcionamiento del Sensor de Ultrasonidos

El sensor de ultrasonidos tiene que tener situados físicamente los dos transductores (el emisor y el receptor) paralelos, y orientados en el mismo sentido, ya

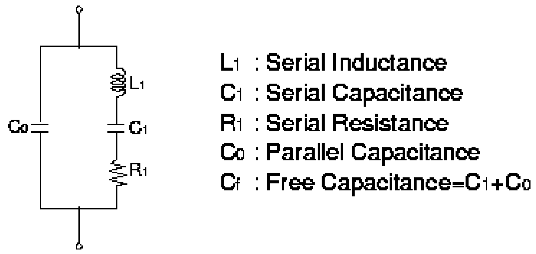

Figura 6.9: Circuito Equivalente de un Transductor piezoeléctrico.

que debido a la frecuencia a la que trabajan, y a su forma son muy direccionales, y una mala colocación reduciría ampliamente el rango de medida.

El sensor de ultrasonidos estará compuesto de dos partes:

Emisor de Ultrasonidos

Este circuito se encarga de generar la señal de 40KHz, así como de un amplificador que excita el transductor piezoeléctrico que hace de emisor, durante un periodo que se le indique desde la parte de control.

Receptor de Ultrasonidos

Este circuito debe recoger la señal del transductor piezoeléctrico que hace de receptor.

Esta señal es amplificada para trabajar sobre ella con mas facilidad.

Luego es filtrada y rectificada, para eliminar el posible eco directo que reciba del emisor.

Por ultimo la señal se convierte a valores lógicos.

Funcionamiento

El circuito que se utiliza en el robot de este proyecto tiene un funcionamiento muy similar al modulo comercial SRF04.

Este circuito tiene dos pines de alimentación, un pin que cuando se activa hace que el emisor de ultrasonidos envíe una señal, y un cuarto pin que se activa cuando se recibe un eco.

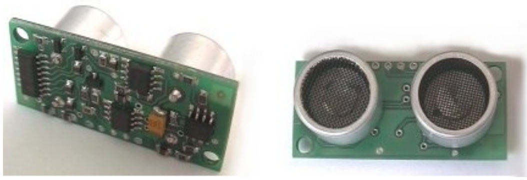

Figura 6.10: Sensor comercial de Ultrasonidos SRF04

Su funcionamiento es el siguiente:

- Se envía un pulso de alrededor de 1 o 2 ms, Ton en la figura 6.11.
- Se espera un tiempo Twait, para evitar posibles falsas medidas debidas a la captación directa del ultrasonido por parte del receptor.
- Tras este espacio, se cuenta el tiempo que tarda en activarse la salida, T en la figura 6.11 y por software conociendo el tiempo se calcula la distancia a la que esta el objeto.

podemos calcular el tiempo que tarda en recorre un cm que es:

$$t = \frac{1s}{170,5m * 100} = 58,65\mu s \tag{6.2}$$

Contando cuantos intervalos de $58,65\mu s.$ tarda la señal obtendremos el valor en centímetros directamente.

6.7.5. Descripción del Circuito Electrónico

Los dos circuitos eléctricos van situados sobre la misma placa de circuito impreso (PCB), y los sensores de ultrasonidos van soldados perpendicularmente a la PCB para reducir el espacio ocupado sobre el robot.

Emisor de Ultrasonidos

Hay un oscilador formado por un circuito integrado NE555 funcionando en modo astable, con un duty cycle cercano al 50 % a una frecuencia de 40KHz. Vosc en la figura 6.11

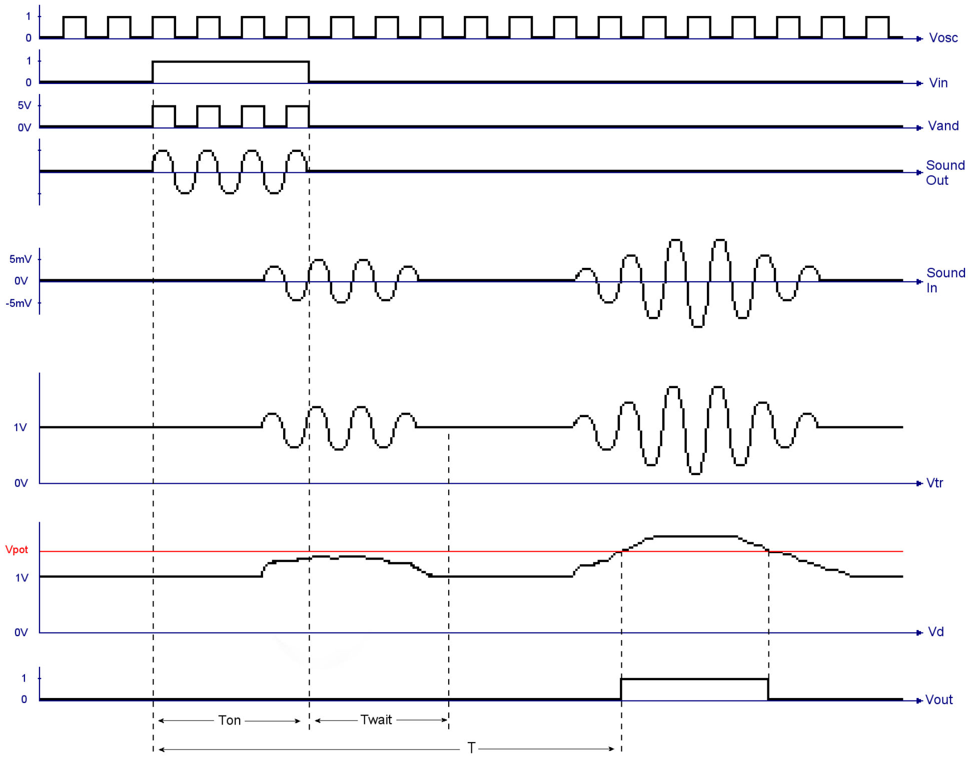

Figura 6.11: Forma de ondas en las distintas partes del sensor.

La señal pasa por un circuito lógico AND, con lo que la salida es 0, salvo en el caso de que desde el circuito de control envíe un 1 (Vin en la figura 6.11), con lo que se obtiene a la salida la señal de 40KHz. Vand en la figura 6.11

Esta señal pasa por 2 inversores (con lo que queda igual) el segundo doble, que actúan como inversores y se reparten el consumo de corriente que puede provocar el transductor, conectado a la salida de estos.

Debido a la alta selectividad de frecuencias, no importa la forma de la señal con que se alimente el transductor, la salida de ultrasonidos sera senoidal. Sound out en la figura 6.11

Receptor de Ultrasonidos

El receptor de ultrasonidos (Sound in en la figura 6.11) alimenta un amplificador realizado con un transistor en modo emisor común, que se ha preferido a los amplificadores operacionales debido a su bajo ruido y gran ganancia. Vtr en la figura 6.11

La señal amplificada pasa por un diodo que rectifica y filtra (gracia a la capacidad parásita del diodo) la señal, obteniendo una señal continua con la forma de la señal recibida. Vd en la figura 6.11

Un Amplificador operacional actuando como comparador convierte la señal en cuadrada, que luego pasa por dos inversores que la convierten en TTL sin modificarla. Vout en la figura 6.11

6.8. El Microbot

Debido a la naturaleza del robot, no es necesario un control preciso sobre la velocidad de giro de los motores, por lo que este robot no tiene ningún sistema de sensores de realimentación sobre el funcionamiento de los motores.

El robot incorpora cuatro sensores iguales de ultrasonidos, tres apuntando hacia adelante cubriendo la zona de movimiento normal del robot, y uno hacia atrás.

Estos sensores son tontos, simplemente encargándose de emitir una señal de ultrasonidos, y convertir la señal de vuelta a niveles TTL para poder procesarlos con el microcontrolador.

Capítulo 7

Sistemas de Control

Es necesario un sistema que una todas las partes vistas anteriormente y lo haga funcionar, es lo que llamaríamos el "cerebro" del robot, y es lo que hará que el robot racione de una determinada manera.

7.1. Lógicos

Es el sistema mas simple de control, basados en las funciones lógicas AND, OR y NOT, bien por lógica basada en interruptores, , bien por puertas lógicas digitales, y permiten al robot tomar decisiones simples ante estímulos exteriores que recibe por sensores.

Mediante este sistema solo es posible hacer robots "tontos"que pueden resolver problemas limitados.

7.2. Ordenador Remoto

En este caso los sensores y sistemas de tracción están controlados por un ordenador, normalmente mediante un lenguaje de alto nivel de facilita la tarea, la comunicación suele ser por medio de un cable, o un sistema inalámbrico, y permite la realización de operaciones muy complejas como algoritmos de inteligencia artificial, o reconocimiento visual, con la desventaja de necesitar un ordenador unido por algún sistema al robot.

Con los avances de la técnica, y la actual proliferación de sistemas "embebed" o empotrados y SBC (single board computer) cada vez es mas habitual ver robots donde el ordenador no es remoto, si no que va incluido en el propio robot.

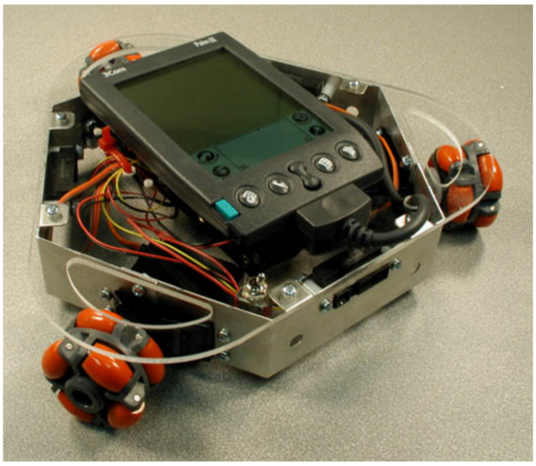

Figura 7.1: Este microbot es controlador por un ordenador de bolsillo Palm Pilot

7.3. Microcontrolador

Entre los dos sistemas anteriores, cuando no se necesita la potencia de un ordenador, se encuentras los microcontroladores, que evitan la necesidad de un ordenador Host, y permiten resolver problemas mas complicados que los que permitiría la lógica cableada.

Un microcontrolador incorpora en un simple chip, un completo ordenador, en ocasiones con una potencia muy superior a los típicos microordenadores de los años 80 y principios de los 90.

Suele incorporar Memoria RAM, Memoria ROM, la propia CPU, y suele disponer de muchas patillas configurables como entradas o salidas (a diferencia de los microprocesadores nacionales que suelen compartir las funciones de las patillas y necesitar lógica adicional).

La mayoría de los fabricantes poseen un amplio rango de microcontroladores, de diversas potencias (rangos de frecuencia de trabajo y nº de bits) y cantidad de patillas de I/O, además de circuitos adicionales, en muchos casos los modelos superiores son compatibles en patillaje o código con los inferiores, permitiendo una ampliación del sistema cuando este se queda pequeño.

Existen varios fabricantes de microcontroladores, como Zilog con la serie Z, philips con la serie 80C32 e Intel con la serie 8051, aunque no son muy utilizados en microrobotica, entre los mas utilizados destaca:

7.3.1. Motorola HC11

Probablemente uno de los primeros en aparecer en escena, esta basado en la arquitectura de microprocesador MK68K, arquitectura Von Newman, y RISC (Reduced Instruncions Set Code, reducido numero de instrucciones), con registros de memoria.

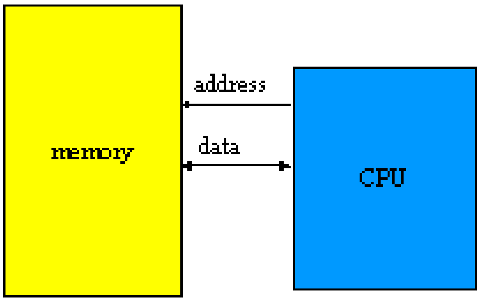

Figura 7.2: Arquitectura Von Neumann, Datos y Programa Juntos.

Es ampliamente utilizado en EEUU, donde los ordenadores basados en la familia M68K (como los apple macintosh) tiene gran tradición.

Uno de sus inconvenientes es que prácticamente solo el fabricante proporciona herramientas de desarrollo y estas tienen un coste elevado, lo que limita la experimentación amateur con el mismo.

7.3.2. Atmel AVR

Históricamente el ultimo en ser utilizado en la escena de microbots, esta fabricante posee dos ramas de microcontroladores, una basada en el Intel 8051, que a su vez esta basado en los 8080, y otro propio el AVR con arquitectura Von Newman, RISC, y registros en el microprocesador, destaca por ser mas barato que el pic, y tener herramientas de desarrollo libres, algunas de ellas de lenguajes de alto nivel como el BASIC o el C, la interfaz necesaria para programarlo es barata y de fácil construcción, lo que permite una inversión inicial mínima.

7.3.3. Microchip PICmicro

Este microcontrolador se aleja de lo tradicional, Tiene una arquitectura Harward, RISC y registros en memoria, incorpora ciertas mejoras, como un pipeline que le permiten ser mucho mas rápido, hasta una instrucción por ciclo de reloj, existiendo clones fabricados por otras marcas (como los scenix) con velocidades mucho mas altas que las del fabricante microchip.

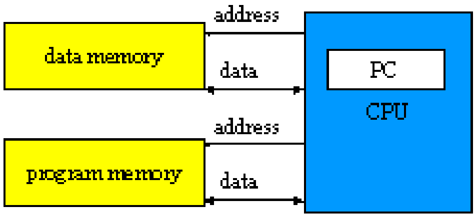

Figura 7.3: Arquitectura Harward, Datos y Programa en buses independientes.

El fabricante proporciona una cantidad de información significativamente mayor que el resto, así como Herramientas Software para programarlo, existe también una amplia cantidad de Herramientas de terceros, y al igual que el AVR posee una interfaz de programación muy sencilla, permitiendo incluso la programación una vez soldado al circuito impreso.

7.4. El microcontrolador PICmicro 16F84A

El modelo 16F84A esta en lo que el fabricante denomina ”mid-range”, entre sus características destacan:

- Arquitectura RISC, solo tiene 35 instrucciones de código máquina, excepto las instrucciones de salto, todas se ejecutan en un ciclo de reloj.
- Velocidad de operación de hasta 20MHz.
- Memoria de programa Flash de 1K, el bus de instrucciones es de 14 bits, es programable sobre el circuito utilizando únicamente 2 pins, programable hasta 10.000 veces.
- 68 bytes de memoria RAM, el bus de datos es de 8 bits.
- 64 bytes de memoria EEPROM no volátil, permitiendo hasta 10.000.000 de ciclos de escritura manteniendo su contenido durante 40 años
- 8 niveles de stack para subrutinas (en memoria independiente).

- Tres modos de direccionamiento y cuatro modos de interrupción
- 13 patillas configurables como entradas o salidas, pueden proporcionar 25mA cada una, permitiendo alimentar Leds directamente.

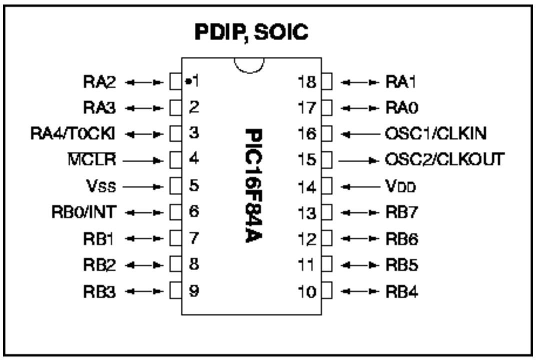

Figura 7.4: Distribución de las patillas del 16F84A

- Temporizados de 8 bits con preescaler de 8 bits.
- Sistema para reset automático al encendido, encendido por timer, y retraso al encendido por oscilador.
- Watchdog Timer con oscilador propio dentro del chip.
- Protecion del código contra lectura.
- Varios tipos de Osciladores.
- Bajo consumo, menor de 2mA trabajando a 4MHz, $0{,}5\mu A$ en modo suspendido y $15\mu A$ trabajando a 32KHz.
- Varios encapsulados disponibles
- tiene 1Kb de memoria flash de programa, lo que permite reprogramarlo cuantas veces sea necesario, 256 bytes de memoria volátil de datos y 384 bytes de eeprom, lo que permite almacenar y conservar calibraciones, y datos incluso en ausencia de energía.

7.4.1. Visión General

El 16F84A se encuentra en la gama “mid-range” de dispositivos del fabricante microchip, se puede observar en la figura 7.5 el diagrama de bloques del microcontrolador.

Dispone de 13 patillas de I/O configurables cada una por separada, además están multiplexadas con otras funciones:

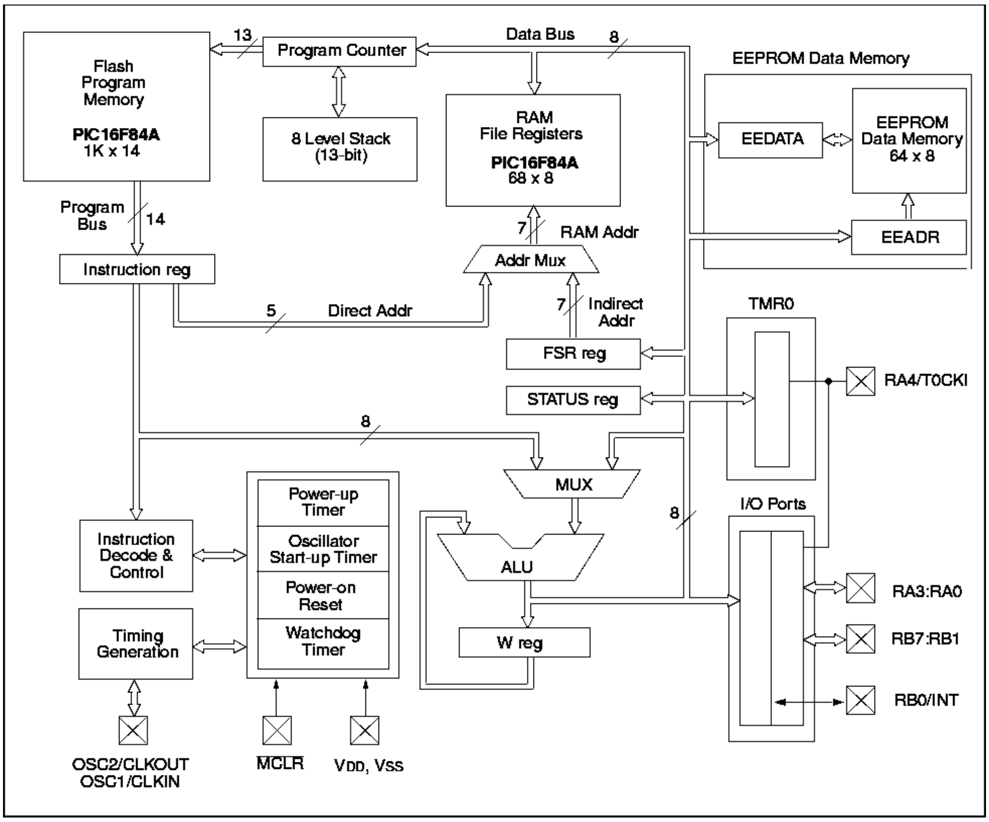

Figura 7.5: Diagrama de Bloques del 16F84A

- Interrupciones Externas
- Interrupciones cuando cambie el puerto B
- Entrada de reloj para el Temporizador 0

En el cuadro 7.1 puede verse la descripción completa de cada patilla.

Nombre de Patilla	PDIP Nº	soic nº	ssop nº	i/o/p clase	Buffer Clase	Descripción
OSC1/CLKIN	16	16	18	I	ST/CMOS	Entrada del oscilador de cristal / Entrada de reloj externa.
OSC2/CLKOUT	15	15	19	O	-	Salida del oscilador de cristal, Conectada a un cristal o resonador cerámico en modo de Oscilador de Cristal. En modo RC la patilla OSC2 saca CLKOUT que es 1/4 la frecuencia de OSC1 y marca el ritmo del ciclo de instrucciones.
$\overline{\text{MCLR}}$	4	4	4	I/P	ST	Reset principal, entrada. Entrada del voltaje de programación, este pin activa el RESET con un cero lógico.
RA0	17	17	19	I/O	TTL	PORTA es un puerto de E/S bidireccional.
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Puede ser seleccionada como entrada de reloj del temporizador contador TMR0. Salida de colector abierto.
						PORTB es un puerto de E/S bidireccional. como entrada pueden activarse por software resistencias de Pull-Up en todas las patillas.
RB0	6	6	7	I/O	TTL/ST	Puede ser utilizada como entrada de interrupccion externa
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupción por cambio.
RB5	11	11	12	I/O	TTL	Interrupción por cambio.
RB6	12	12	13	I/O	TTL/ST	Interrupción por cambio. Reloj en programación serie.
RB7	13	13	14	I/O	TTL/ST	Interrupción por cambio. Datos en programación serie.
Vss	5	5	5,6	P	-	Referencia de tierra para lógica y E/S.
Vss	14	14	15,16	P	-	Alimentación positiva para lógica y patillas de E/S.

Cuadro 7.1: Descripción de cada patilla

7.4.2. Organización de Memoria

La memoria del PIC esta organizada en dos bloques, cada uno de ellos con buses separados, lo que permite acceder a ambos en un único ciclo de reloj.

La memoria de datos puede dividirse en la memoria de propósito general y los registros de funciones especiales (SFRs) que es utilizada para controlar los diferentes periféricos y características del PIC.

En la memoria datos también esta incluía la memoria EEPROM aunque solo se puede acceder a ella mapeada indirectamente.

Organización de la Memoria de Programa

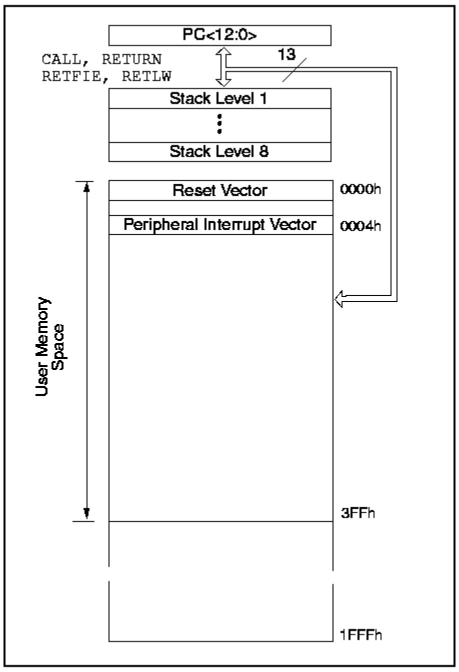

Figura 7.6: Memoria de Programa (ROM)

Los pic 16FXX tienen un contador de 13 bits y pueden direccionar hasta 8K de 14 bits de espacio de memoria, el 16F84A tiene solo el primer 1K (0000h-03FFh) físicamente implementado (figura 7.6) y si se intenta acceder a otras posiciones de memoria se accede al las primeras posiciones, ignorando los bits de dirección que no se usan.

El vector de reset esta en la posición 0000h y el vector de interrupción esta en la posición 0004h.

Organización de la Memoria de Datos

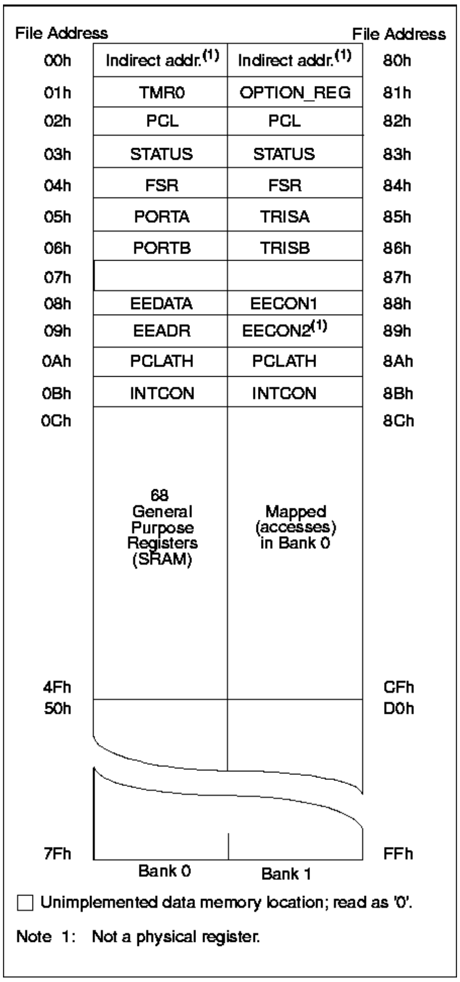

Figura 7.7: Memoria de Datos (RAM)

La memoria de datos es de 8 bits.

La memoria de datos esta dividida en dos áreas, los registros de función especial y los registros de propósito general.

Además la memoria de datos esta en bancos, para permitir superar el limite de 116 registros de propósito general.

En cada banco los 12 primeros registros están reservados a la SFR.

El cambio de banco esta controlado por el bit RP0 del registro STATUS

Se puede acceder a cualquier posición de memoria directamente, o indirectamente a través de la SFR.

Ciertos registros (status, PCL, el registro de acceso indirecto) están duplicados en todos los bancos.

En el 16F84A como solo hay 68 registros de propósito general, están mapeados hasta la posición 4Fh, y están mapeados también en el segundo banco de memoria.

7.4.3. Registros de Función Especial (SFR)

Los registros de función especial son utilizados por la CPU para controlar el funcionamiento del dispositivo, y están situados en la RAM estática.

Podemos dividirlos en dos grupos, los del núcleo, y los periféricos.

trataremos ahora los del núcleo y haremos referencia a los otros cuando tratemos los periféricos.

Registro de Estado (STATUS)

Controla el estado de la ALU, de los bancos de memoria y de la función de RESET.

Este registro puede ser accedido como otro cualquier pero ciertos bits responden al resultado de la operación, entre ellos Z, DC y C, además $\overline{\text{TO}}$ y $\overline{\text{PD}}$ no son escribibles, así la orden `CLRF STATUS`, pondría los tres bit superiores a cero, activaría Z y dejaría los otros sin cambiar.

Únicamente `CBF, BSF, SWAPF` y `MOVWF` deberían ser utilizadas para cambiar el registro de estado ya que no afectan a ningún bit del registro.

Registro de Opciones (OPTION)

Este registro es leíble y escribible y controla ciertas opciones de configuración del preescaler del Temporizador y WDT, las resistencias de Pull-Up del puerto B y la generación de interrupciones INT.

Registro de Control de Interrupciones (INTCON)

Este registro es leíble y escribible y controla las diferentes opciones de interrupción que tiene el microcontrolador y su activación.

Contador de programa (PCL y PCLATH)

El contador de programa (PC) tiene 13 bits de ancho, los bit inferiores son accesibles a través de PCL, los bits superiores no son accesibles y solo pueden ser modificados a través de PCLATH.

Cuando una instrucción de programa genera un salto, este toma dos ciclos de reloj, en el primero se ejecuta la instrucción y en el segundo se ejecuta un NOP mientras el pipeline se recarga con la siguiente instrucción.

Stack

El stack permite que una combinación de hasta ocho llamadas a subrutinas o interrupciones puedan tener lugar simultáneamente. El stack guarda la dirección de retorno para continuar la ejecución del programa.

Este stack esta implementado en hardware, no es accesibles y es cíclico (una novena llamada sobreescribiría la dirección de retorno de la primera).

EL PC es almacenado en el stack al ejecutar la orden `CALL` y es devuelto del STACK cuando se ejecuta `RETURN, RETLW` o `RETFIE`.

Acceso Indirecto a Memoria (INDF y FSR)

INDF no es un registro físico, cualquier lectura o escritura que se haga en el, en realidad se realiza sobre el registro cuya dirección esta en FSR, a esto se le llama Direccionamiento Indirecto.

Intentar leer INDF indirectamente devuelve 00h, escribir en INDF resulta en la ejecución de NOP y la actualización de los bits de estado que sean necesarios.

7.4.4. Memoria EEPROM

El 16F84A incorpora 64 bytes de memoria EEPROM, el acceso a esta memoria se realiza a través de los registros EECON1, EECON2, EEDATA y EEADR, y requiere una secuencia de instrucciones especifica para acceder a ella.

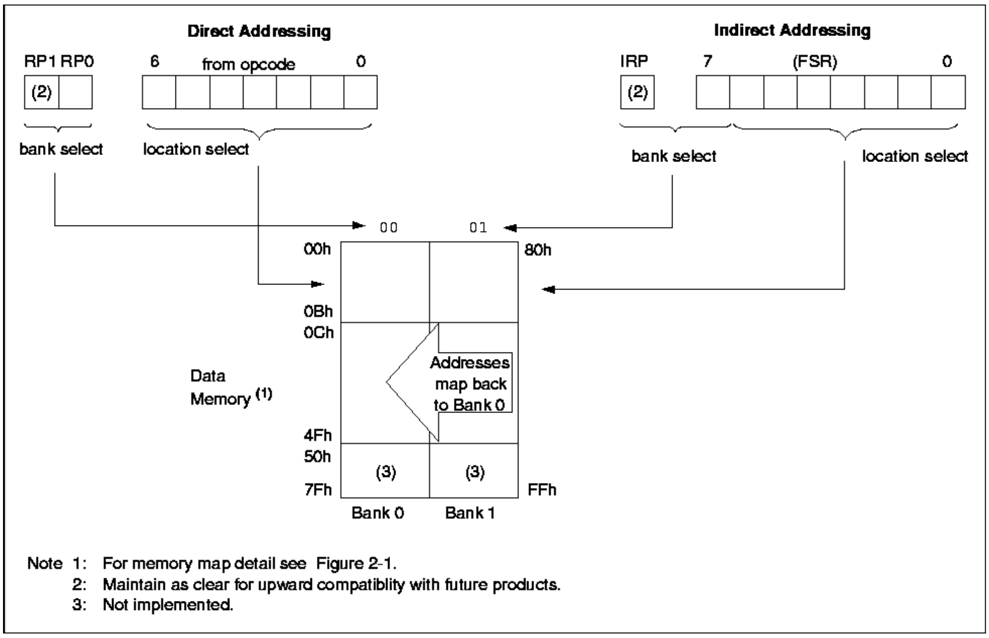

Figura 7.8: Acceso a memoria directo e indirecto

Debido a que esta característica no es utilizada en el proyecto, no se entrara en detalles sobre su funcionamiento.

7.4.5. Puertos de I/O

Algunas patillas de I/O están multiplexadas con funciones alternativas, cuando estas funciones están activadas, no es posible utilizar la patilla como I/O

Puerto A (PORTA y TRISA)

El puerto A de 5 bits de ancho es bidireccional, la dirección de cada bit es controlada por el registro TRISA, poner un bit a 1 en TRISA hace que el bit correspondiente de PORTA funcione como entrada (esto es, pone el latch de salida de esa patilla en alta impedancia), poner un 0 hace que se comporte como salida, poniendo el valor del latch en la patilla.

Leer el registro PORTA lee el estado de los bits, sin importar que funcionen como entrada o salida, todas las operaciones de escritura al puerto son operaciones de lectura-modificación-salida, hay que tener precaución en esto cuando se manejen varios pines como entradas y salidas simultáneamente.

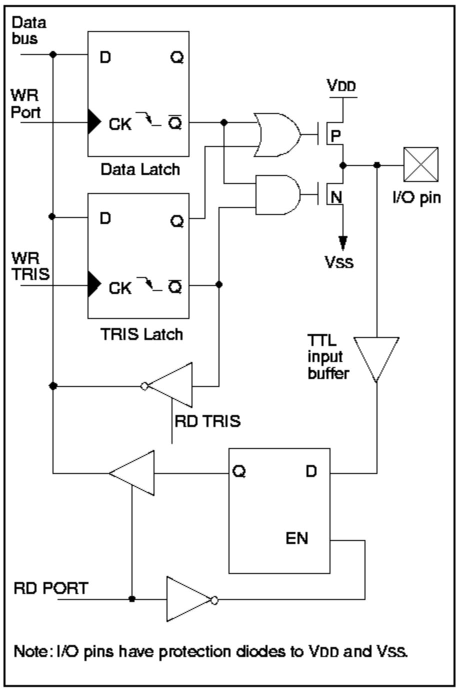

Figura 7.9: Diagrama de bloques de los pines RA3:0

El pin RA4 esta multiplexado con la entrada de reloj del modulo temporizador, la entrada del RA4 es un Trigger Schmitt y la salida en modo colector abierto, el resto de pins de ese puerto tienen entradas TTL y salidas CMOS.

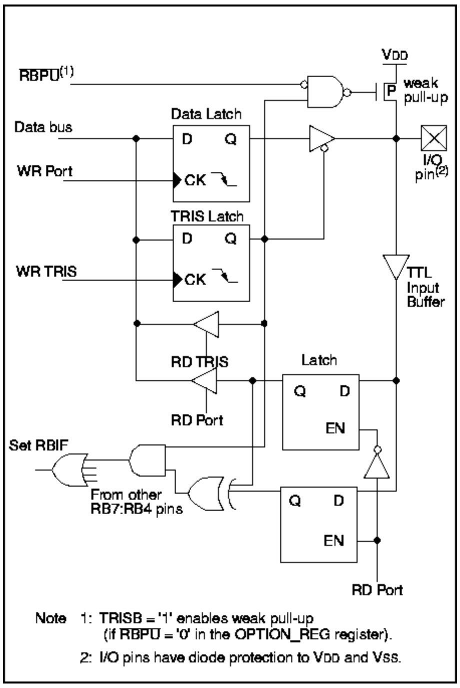

Figura 7.10: Diagrama de bloques del pin RA4

Puerto B (PORTB y TRISB)

El puerto B es de 8 bits de ancho, bidireccional, su registro de datos es PORTB y se controla desde el registro TRISB, de manera idéntica al puerto A, un bit a 1 en TRISB hace que el bit correspondiente funcione como entrada, y un 0 como salida.

Cada pin del puerto B tiene una resistencia de Pull-Up, que son activadas (todas) poniendo a cero el bit $\overline{\text{RBPU}}$ del registro STATUS, esta resistencia es desactivada automáticamente cuando el puerto es configurado como salida, estas resistencias están desactivadas tras el reset de Encendido (Power-On Reset)

Los cuatro bits superiores del puerto, RB7:RB4 tienen la característica de poder generar una interrupción ante un cambio solo si están configurados como entradas. Su valor es comparado con el valor de la ultima lectura del puerto B y si son diferentes activa el bit RBIF del registro INTCON.

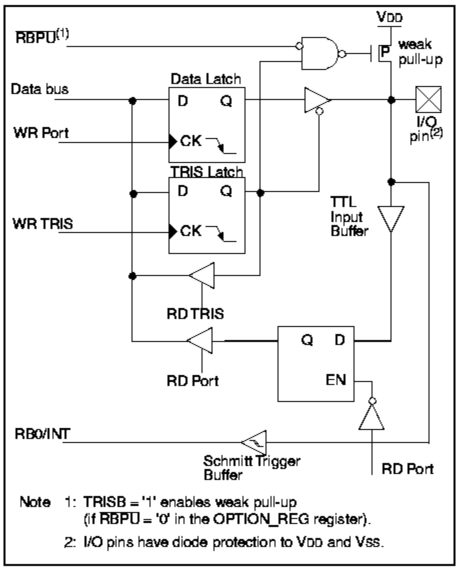

Figura 7.11: Diagrama de bloques de los pines RB3:0

El bit de RBIF es activado siempre que exista una diferencia entre la ultima lectura, una rutina de servicio que gestione esta interrupción debería primero leer el puerto B y después borrar RBIF, pues se volverla a activar si el valor siguiese siendo diferente al de la ultima lectura efectuada.

Esta interrupción puede ”despertar.ªl dispositivo del modo suspendido.

Esta característica de Interrupción al cambio, permite crear teclados con la función de despertar.

No es recomendable sondear el puerto B mientras se utiliza la función de Interrupción al cambio.

7.4.6. Temporizador

El modulo temporizador/contador Timer0 tiene las siguientes características:

- Contador/temporizador de 8 bits, legibles y escribibles.
- Señal de reloj seleccionable interna o externa.
- Flanco de la señal externa seleccionable.
- Preescaler seleccionable de 8 bits.

- Interrupción por rebase de 0xFF a 0x00

En la figura 7.12 puede verse un diagrama del modulo Timer0

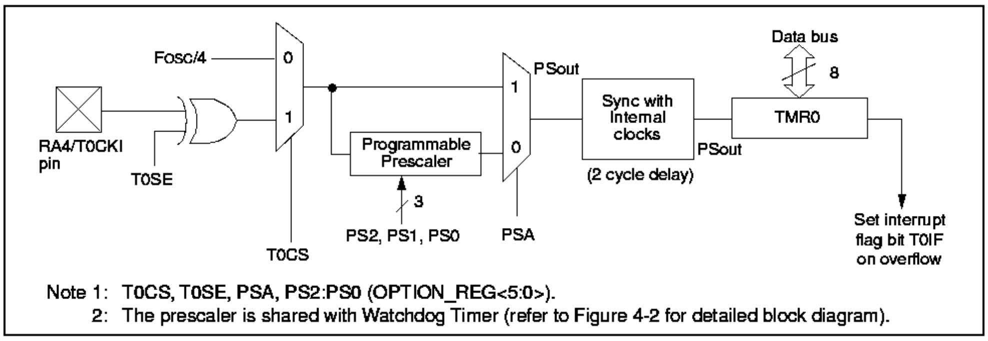

Figura 7.12: Diagrama de bloques del Temporizador

Funcionamiento

EL funcionamiento como contador o temporizador se selecciona con el bit T0CS del OPTION_REG, en modo temporizador el modulo se incrementara con cada ciclo de instrucción (sin preescaler). Si se escribe en el registro del contador, el incremento es anulado en los siguientes dos ciclos de instrucción. esto hay que tenerlo en cuenta a la hora de escribir valores en este registro.

Si se selecciona el modo contador, el registro se incrementara con cada flanco ascendente o descendente (en función de T0SE de OPTION_REG) de RA4/T0CLK.

Cuando se utiliza el reloj externo, la señal debe ajustarse a ciertos valores, para asegurar que se sincronice con el reloj interno, además hay un retraso entre el incremento del registro después de la sincronización.

Preescaler

Un contador de 8 bits esta disponible como preescaler para Timer0, o como postescaler para el Temporizador Watchdog, no puede ser utilizado por los dos módulos a la vez.

Este contador no esta disponible para el usuario, su asignación y valor se controla con los bits PSA y PS2:PS0 de OPTION_REG.

Los valores seleccionables están entre 1:1 y 1:128, además para el Timer0 puede seleccionarse también el valor de 1:256.

Cuando se asigna a Timer0 cualquier instrucción que escriba el registro de Timer0 pondrá a cero el preescaler, cuando se asigne al watchdog la instrucción `CLRWDT` pondrá a cero el preescaler.

Interrupción

cuando el registro de Timer0 rebasa el valor 0xFF pasando a 0x00 se produce una interrupción TMPR0, puede ser enmascarada poniendo a cero el bit T0EI de INTCON. La interrupción activa el bit T0IF de INTCON, este bit debe ser puesto a cero por software en la rutina de servicio de la interrupción antes de volver a activar las interrupciones, esta interrupción no puede despertar al microcontrolador de SLEEP ya que durante este periodo el temporizador se apaga.

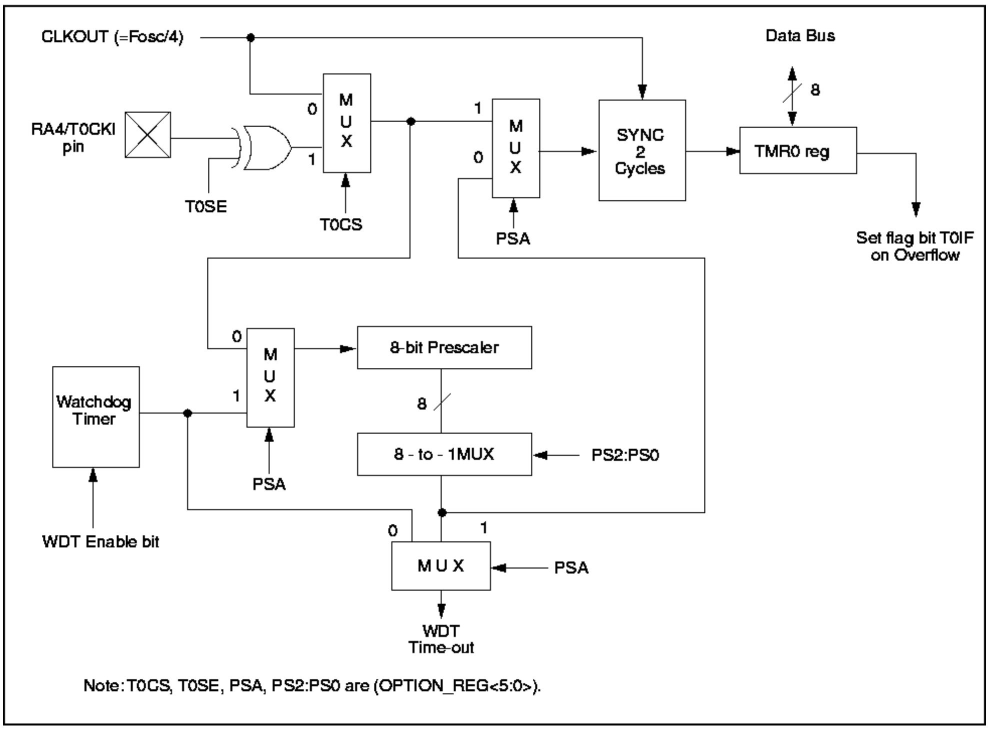

Figura 7.13: Diagrama de bloques del prescaler

7.4.7. Funciones Especiales

Una de las características que diferencia este microcontrolador de otros son sus funciones especiales, enfocadas a aumentar su flexibilidad o fiabilidad.

Bits de configuración

Una posición de memoria solo accesible durante la programación (0x2007) permite seleccionar que funciones especiales se van a utilizar en el microcontrolador.

Oscilador de Reloj

Es posible controlar el reloj del microcontrolador de cuatro maneras:

- LP Cristal de cuarzo de baja potencia.
- XT Cristal de cuarzo o resonador cerámico
- HS Cristal de cuarzo o resonador cerámico de alta velocidad
- RC Resistencia-Condensador

En la hoja de características del Microcontrolador pueden encontrarse esquemas tipo de como debe ser el circuito de oscilación, así como tablas con los valores recomendados para cada oscilador.

En los modos HS, XT o LP se puede utilizar un oscilador externo, conectado a OSC1, quedando OSC2 sin conectar.

El oscilador RC proporciona una opción barata para aquellas aplicaciones que no sean sensibles a la temporización, ya que los osciladores RC varían su frecuencia con la temperatura, tolerancias de los componentes y tensión de alimentación.

Reset

El microcontrolador diferencia entre cinco modos diferentes de reset:

- Reset al encendido (Power-On Reset).
- $\overline{\text{MCLR}}$ durante funcionamiento normal.
- $\overline{\text{MCLR}}$ durante SLEEP.
- Reset del WDT durante funcionamiento normal.
- Despertar del WDT durante SLEEP.

En función de cada uno de estos tipos de reset, la ejecución del programa continua en una determinada dirección, y varios registros cambian de valor, lo que permite al programa identificar el tipo de reset que se ha producido.

En la hoja de características del microcontrolador se encuentra una lista completa de todos los registros afectados en cada situación.

Reset al Encendido

Se produce cuando se detecta una subida en el valor de Vcc (entre 1.2v y 1.7v), para lo cual es necesario que la patilla $\overline{\text{MCLR}}$ este llevada directamente a Vcc (o como mucho a través de una resistencia) y permite eliminar las redes RC que normalmente se ponen para asegurar el correcto encendido del micro.

Temporizador de encendido

Un retraso fijo de aproximadamente 72ms (dependiendo de factores externos como temperatura, el propio chip, etc. . .) en el encendido que puede ser activado mediante un bit de configuración.

Este temporizador cuenta con su propia red RC, y mantiene al chip en RESET mientras dure la temporización, permite esperar a que el valor de Vcc alcance un valor estable antes de empezar a funcionar.

Temporizador de encendido del Oscilador

Es un retraso de 1024 ciclos de reloj que se produce al salir de SLEEP o en un Power-On, en las configuraciones de XT, LP o HS y permite asegurar la estabilidad del oscilador antes de empezar a ejecutar el programa.

Estado tras el encendido

EL microcontrolador dispone de dos bits $\overline{\text{TO}}$ y $\overline{\text{PD}}$ que permiten saber la razón por la que se ha producido un reset, y así distinguir un reset normal, de uno producido por el watchdog timer.

Del mismo modo permiten determinar si el volver del modo suspendido, se produjo por el watchdog timer, por una interrupción o por utilizar la patilla de e reset $\overline{\text{MCLR}}$.

Esta opción no se utiliza en el proyecto.

Interrupciones

El microcontrolador dispone de cuatro interrupciones enmascarables:

- Interrupciones externa en RB0/INT
- Rebase del Timer0
- Cambio en el puerto B
- Escritura completada en la EEPROM interna

Son controladas por el Registro INTCOM, tiene un bit general de enmascaramiento GIE, y cuatro para cada una de las interrupciones.

Existe además la instrucción `RETFIE` que retorna de una función y vuelve a activar las interrupciones.

Cuando se produce una interrupción PC es guardado en el stack se desactivan las interrupciones y se salta a la posición de memoria 0x004, las interrupciones tienen una latencia de entre tres y cuatro ciclos de instrucción.

Cada interrupción tiene un bit que permite a la rutina determinar cual de las interrupciones se ha producido.

Estos bit se activan aunque las interrupciones estén anuladas, lo que permite a la rutina de control de interrupciones responder a varias interrupciones a la vez, o a interrupciones que se produzcan mientras de atiende a otras.

Guardar el estado durante las interrupciones

Cuando se produce una interrupción únicamente el valor de PC se almacena en el stack, es necesario reservar dos registros W_TEMP STATUS_TEMP y seguir una secuencia exacta de instrucciones en la rutina de respuesta a las interrupciones para asegurar que al final de la rutina de interrupción se vuelve al estado que existían antes de que se produjese.

Temporizador Watchdog

El microcontrolador dispone de un temporizador y un oscilador RC independiente del resto del chip, que provoca un RESET al cabo de un tiempo determinado si no es desactivado o puesto a cero cada cierto tiempo (aproximadamente 18ms sin preescaler), lo que permite aumentar la fiabilidad p.e. provocando un reset automático si el programa se bloquea y asegurando la respuesta del sistema, o un funcionamiento con muy bajo consumo combinado con la opción de modo suspendido.

Esta opción no se utiliza en el proyecto.

Modo suspendido

El microcontrolador dispone de un modo de bajo consumo de energía SLEEP durante el cual se suspende todo el funcionamiento de micro.

De este modo se puede sacar al microcontrolador de varias maneras, mediante reset, el watchdog o por interrupciones externas.

Esta opción no se utiliza en el proyecto.

Protección o verificación del programa

En función de los bits de configuración, el programa podrá ser extraído del microcontrolador, p.e. para comprobar que ha sido grabado correctamente, o se impedirá su extracción para protegerlo.

Esta opción no se utiliza en el proyecto.

ID Lotacions

El microcontrolador dispone de cuatro posiciones de memoria no accesibles por el programa donde se puede almacenar códigos de comprobación, numeroso de serie u otro valor que pueda interesar verifica mas adelante.

Esta opción no se utiliza en el proyecto.

Programación en el propio circuito

Este microcontrolador permite ser reprogramado sobre el propio circuito y solo requiere dos lineas de datos y tres de alimentación.

Esta opción no se utiliza en el proyecto.

7.4.8. Instrucciones

Este microinterruptor tiene instrucciones de 14 bits que se dividen en el operador y los argumentos de la operación, en la figura 7.14 se muestra una relación de todas las instrucciones disponibles.

Mnemonic,	Operands	Description	Cycles	14-Bit Opcode (MSb … LSb)	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 1fff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 1fff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

Figura 7.14: Set de instrucciones del PIC16F84A

En ellas f representa el registro de memoria y d representa el destino de la operación, si es 0 el resultado se almacena en W y si es uno el resultado se almacena en el registro de memoria.

k representa un valor constante (de 8 o 11 bits) utilizado en la operación.

Todas las instrucciones son ejecutadas en un solo ciclo de instrucción, excepto cuando una instrucción de comprobación es correcta o se modifica PC, entonces la instrucción toma 2 ciclos de reloj, en el segundo se ejecuta NOP mientras se recargan los pipelines del microcontrolador.

Un ciclo de instrucción son cuatro ciclos de reloj, por lo que si se opera a una frecuencia de 4Mhz cada instrucción tarda $1\mu s$ en ejecutarse.

7.5. El Microbot

El control del robot se realiza mediante un microcontrolador PIC 16F84A, que se encarga de procesar las señales de los sensores, hacer los cálculos de distancias, evaluar las posibilidades y enviar las ordenes a los driver de los motores.

El puerto A del microcontrolador sera utilizado para controlar el driver de los motores.

El puerto B es utilizado para controlar los sensores, los 4 bits inferiores par la salida de señal, y los cuatro superiores (aprovechando la posibilidad de generar interrupciones) para la recepción de la señal.

Tendrá un oscilador basado en cristal de cuarzo, y no incorpora circuito de reset, aprovechando la facilidad de “power on reset” de este chip.

Capítulo 8

Descripción de los Circuitos Impresos

El robot esta compuesto por cinco placas de circuito impreso, una principal, donde esta la parte de energía, control y los drivers para los motores, y cuatro iguales, una para cada sensor de ultrasonidos.

Cada uno de los circuitos de sensores va unido a la placa central por medio de un conector de 4 conexiones en linea, este conector solo tiene una posición, y se utiliza un código de cables de colores para evitar colocarlo erróneamente.

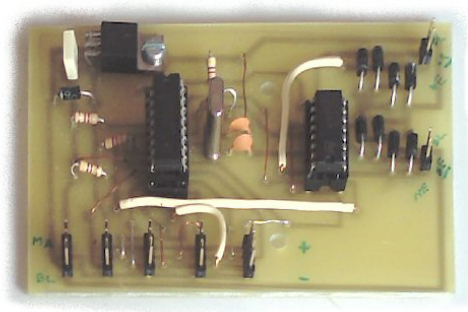

Figura 8.1: Placa Principal terminada.

8.1. Placa Principal

La placa principal va sujeta a la plataforma inferior por tres separadores de circuito impreso de media pulgada, sobre unos agujeros roscados que existen en ella.

En la figura 8.2 se puede observar el diagrama de bloques de la placa principal que consta de:

Un Circuito de alimentación y estabilización, que se encarga de suministrar dos fuentes de energía, una para los motores, que esta sin estabilizar, y otra para el microcontrolador y los integrados, que esta estabilizada en 5V. para asegurara el funcionamiento correcto del microcontrolador.

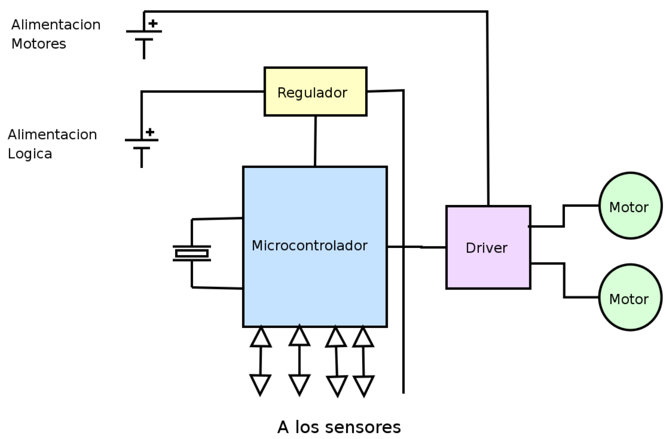

Figura 8.2: Diagrama de bloques de la placa principal

Un Driver, que se encarga de suministrar la potencia a los motores, a la vez de aislarlos del resto del circuito y que es manejado por el microcontrolador.

Un microcontrolador, alimentado por el estabilizador, gobierna el driver de los motores y controla los sensores de ultrasonidos, a los que envía y recibe información, que procesa y evalúa para determinar las ordenes a enviar al driver.

Analicemos cada una de las tres secciones:

8.1.1. Circuito de Alimentación

Las dos tensiones son suministradas a través de un interruptor doble que incorpora la base del robot, encendiéndolas o apagándolas a la vez con una sola palanca.

La tensión de los motores pasa directamente al circuito del driver del motor.

El circuito de alimentación lo forma un integrador LM7805 que estabilizara la tensión de 9V de una de las baterías y que alimentara los integrados y sensores, incorpora un condensador de filtro de las posibles interferencias que causasen

Figura 8.3: Detalle de Regulador de Tensión

los integrados, y un diodo, trabajando normalmente en inversa, que protege al LM7805 de tensiones inversas que pudiesen producirse, al desconectar la pila y estar aun cargado algún condensador, o generadas por los motores al girar las ruedas manualmente, ya que los LM7805 se estropean muy fácilmente si la tensión de salida supera la tensión de entrada.

El utilizar la tensión ya regulada por parte de los sensores, ahorra en tener que utilizar etapas aisladoras o adaptadoras de nivel entre la señal proporcionada por los sensores, y la requerida por el microcontrolador.

8.1.2. Circuito de Control

Esta formado por el integrado microPIC 16F84A y sus componentes accesorios.

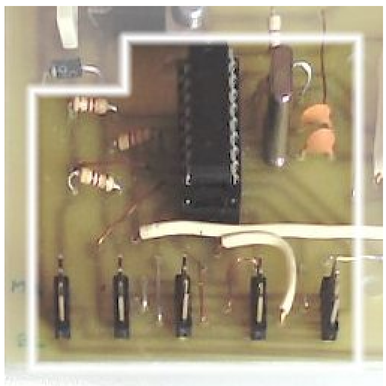

Figura 8.4: Detalle de Microcontrolador y los componentes accesorios

Un cristal de cuarzo de 4MHz y dos condensadores de 27pf que forman el circuito de oscilación, siguiendo las recomendaciones del la hoja de características del producto.

Una resistencia que lleva la patilla MCLR a Vcc forma el circuito de reset, para poder aprovechar la facilidad de Power n Reset de este integrado.

Cuatro resistencias que aseguran a falta de mando del pic que las salidas que controlan los motores están todas a cero, evitando movimientos repentinos e indeseados del robot, estas salidas están conectadas a su vez al driver del motor.

Otras cuatro patillas de entrada y cuatro de salida, así como la tensión rectificada y masa se conectan a cuatro conexiones en la placa, a las que irán cada uno de los cuatro sensores.

8.1.3. Driver del Motor

El driver del motor es un el integrado L293D situado entre el microcontrolador y los motores, formando dos puentes en H, según la configuración que recomienda el fabricante en la hoja de características y Hoja de aplicaciones, este integrado es el único que recibe la segunda tensión de 6V que alimenta los motores, y garantiza el aislamiento entre la parte de potencia y la parte de lógica.

Figura 8.5: Detalle del driver del motor y los diodos de protección

Se han añadido cuatro diodos por motor, tienen como misión proteger al integrado y al resto del circuito de los picos inversos de tensión que se producen en el motor debido a la conmutación de las bobinas.

8.2. Sensor de Ultrasonidos

El robot se compone de cuatro sensores de ultrasonidos, un soporte de madera los sujeta y orienta en cuatro de las posibles direcciones de movimiento del robot, cada uno de estos sensores se compone de una placa de circuito impreso.

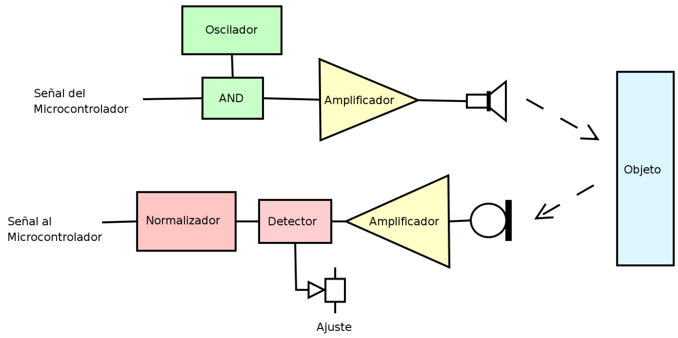

Figura 8.6: Diagrama de bloques del sensor de ultrasonidos

en la figura 8.6 puede verse el diagrama de bloques del sensor de ultrasonidos, en el que destacamos dos partes:

Una parte, que emite los ultrasonidos, esta compuesta por un oscilador, que genera una onda cuadrada de aproximadamente 40KHz, por una puerta lógica AND que hace que solo cuando el microcontrolador lo desea la señal se emita, y un amplificador, que aumenta la potencia de la señal para que pueda ser emitida por la cápsula de ultrasonidos.

Figura 8.7: Placa del Sensor de Ultrasonidos terminada.

El sonido viaja por el espacio, rebota y es devuelto al sensor de ultrasonidos.

En la segunda parte del sensor, otra cápsula capta este sonido, que pasa por un amplificador que convierte la señal a unos niveles mas manejables.

Esta señal pasa después por una etapa detectora, que determinara si hay señal de ultrasonidos, y que tiene la sensibilidad ajustable mediante un potenciómetro.

Por ultimo una etapa normalizadora, convierte el resultado del detector en uno que sea manejable por el microcontrolador.

El Circuito impreso de los sensores esta dividido en dos partes:

8.2.1. Emisor

Un oscilador formado por un 555 en configuración astable, con los componentes necesario para su oscilación, y con un condensador de estabilización C1, tal como recomienda el fabricante en la hoja de características.

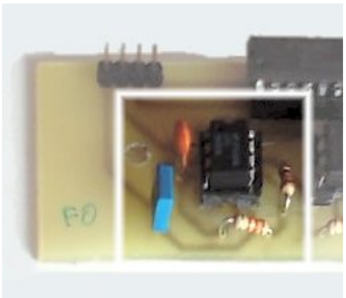

Figura 8.8: Detalle de los componentes del oscilador basado en el 555

Se calcularon los valores de los componentes para obtener:

$$t_1 = 0{,}693(R_1 + R_2)C_1 = 0{,}693(1200 + 33000)560x10^{-12} = 13{,}2x10^{-6} \quad (8.1)$$

$$t_2 = 0{,}693(R_2)C_1 = 0{,}693(33000)560x10^{-12} = 12{,}8x10^{-6} \quad (8.2)$$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{13{,}2x10^{-6} + 12{,}8x10^{-6}} = 38451Hz \approx 40Khz \quad (8.3)$$

Que se acercan al valor de $40000Khz$ deseado, teniendo en cuenta las tolerancias de los componentes.

Un conjunto de una Puerta lógica AND, y tres trigger Smitt inversores, actuando como amplificadores de la señal completan el circuito y alimentan el emisor de ultrasonidos.

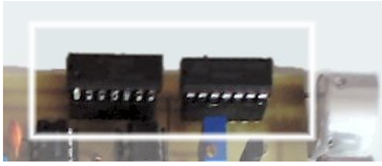

Figura 8.9: Detalle de los chips con la puerta lógica AND y los amplificadores

8.2.2. Receptor

Un amplificador emisor común, recibe del la señal del receptor de ultrasonidos y la amplifica a niveles aceptables para trabajar con ella.

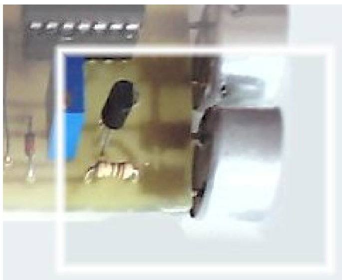

Figura 8.10: Detalle de la cápsula receptora y el amplificador con un transistor

Un diodo actúa como rectificador y convierte la señal recibida una continua y variable en el tiempo en función de la señal.

Un amplificador operaciones TL081 de bajo ruido, actuando como comparador entre la señal que llega del diodo y una de referencia ajustada por el potenciómetro R9, convierte la señal en una onda cuadrada, debido a la alimentación no simétrica del amplificador operacional, y a la tensión de offset, la onda resultante puede no ser valida para utilizar en circuitos integrados TTL y necesita de un ultimo paso.

Por ultimo dos puertas lógicas trigger Smitt inversoras ajustan los niveles para que sean compatibles con TTL y puedan ser procesadas por el microcontrolador.

Capítulo 9

Programa del Microcontrolador

9.1. Descripción General

El programa que controla el robot cumple con los siguientes cometidos:

- Explorar su entorno.
- Decidir que acción realizar en función del entorno.
- Enviar las ordenes adecuadas a los motores para ejecutar la acción.

Para la decisión de la acción a llevar, el robot utiliza una tabla, que esta gráficamente representada en en la figura 9.1 en donde aparece representados los posibles obstáculos que puede encontrar el robot, y la acción a realizar en cada caso.

Esta tabla ha sido estudiada para que el robot se encuentre en constante movimiento y sortee los obstáculos que se encuentre en su camino.

El funcionamiento del programa podemos verlo en el flujograma de la figura 9.2 y que a continuación pasamos a desarrollar.

El programa del microcontrolador podemos dividirla en cuatro partes:

- Inicialización del programa y definiciones.
- Bloque principal.
- Rutina de Lectura de los sensores.
- Rutina de respuesta a las interrupciones.

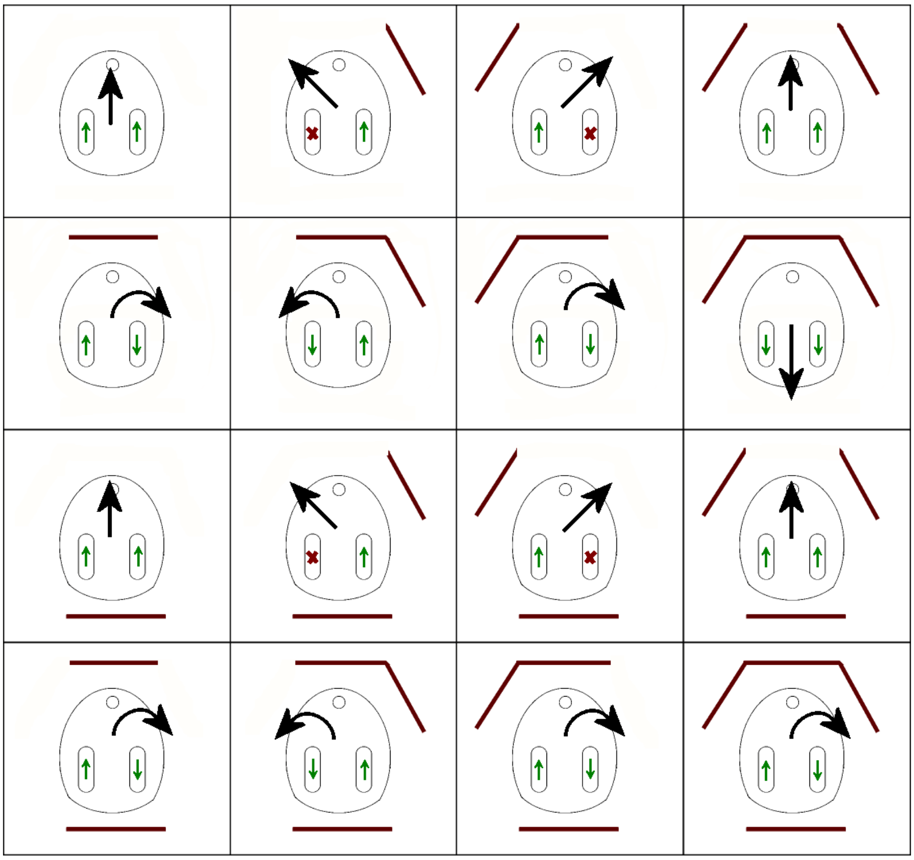

Figura 9.1: Tabla de Decisiones del robot.

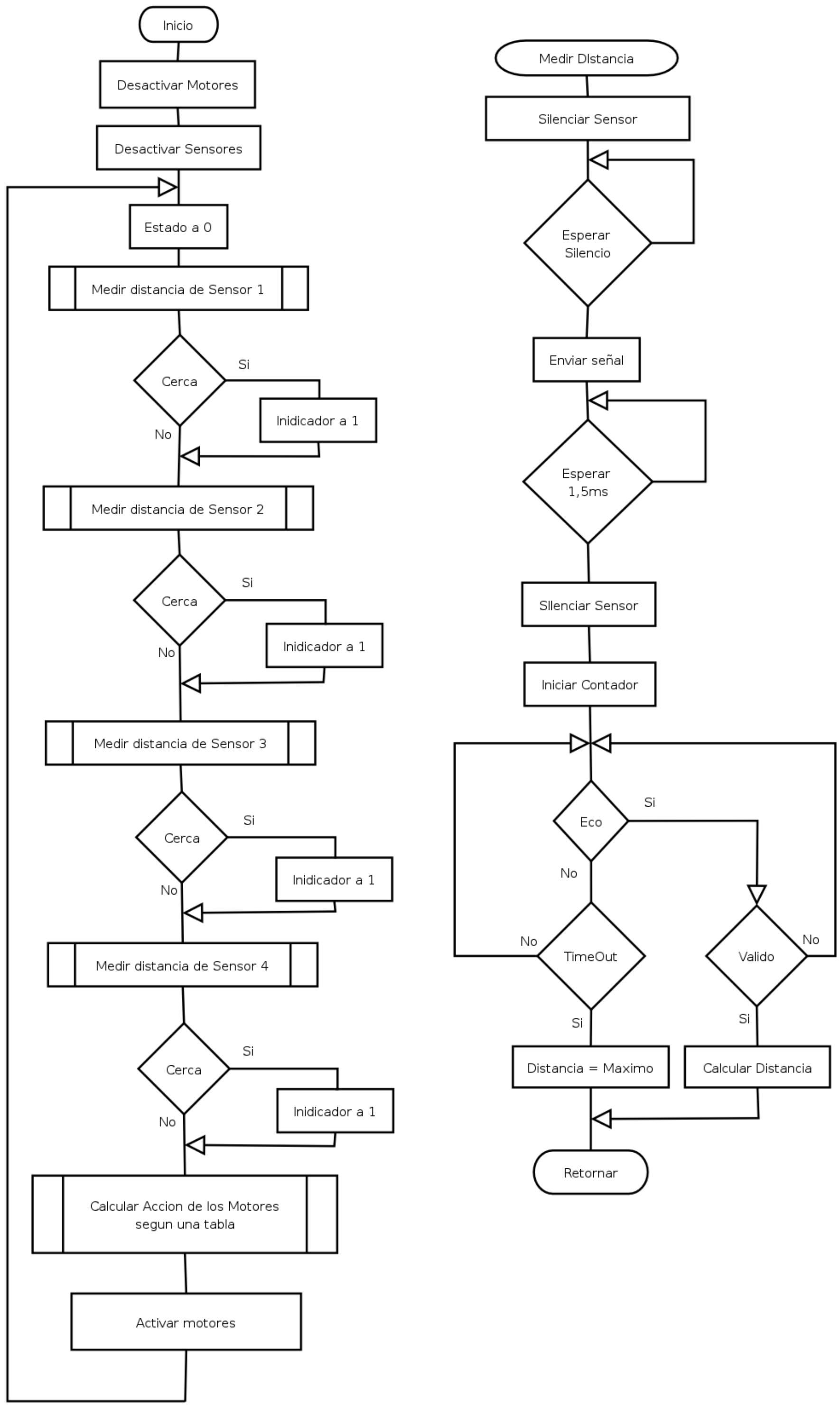

Figura 9.2: Flujograma del programa del microcontrolador.

9.2. Inicialización del Programa y Definiciones

9.2.1. Resumen

En la inicialización se describen las posiciones de memoria y constantes que se van a usar y se inicializa los puertos del microcontrolador.

9.2.2. Descripción

En la primera parte del programa se define las características de funcionamiento del microcontrolador:

- No utiliza el wachtdog.
- Reloj por oscilador de cristal de cuarzo.
- Sin Protección contra lecturas.
- retraso en el encendido (Power-On reset timer).

Se incluyen las ordenes que si bien no afectan al resto del programa, facilitan la tarea, ya que el programador del microcontrolador las lee y no es necesario especificarlas.

Se declaran algunos valores que se utilizaran mas adelante, en concreto unos registros temporales que serán utilizados por la rutina de interrupción, y varios registros que serán utilizados por la rutina de lectura de sensores.

Después se declaran unas constantes que se utilizaran durante el programa: `SensorNo`, `SensorNi` y `SensorNd`, siento `N` el numero de sensor, contienen la patilla de salida, de entrada y el valor máximo (multiplicado por $64\mu S$) de tiempo que tarda el eco en regresar, y que se considera que tiene un objeto cerca, este valor es aproximado al numero de cm.

También se define el máximo valor que puede medir el sensor, puesto arbitrariamente a 64, aproximadamente 64cm.

El programa empieza en la etiqueta inicio donde primero se configura el puerto A como salida (donde están conectados los motores).

Se configura el puerto B, los cuatro bits inferiores como salida y los 4 bits superiores como entrada.

Después de ponen todas las salidas del puerto A a 0 (ningún motor en funcionamiento), y del puerto B (ningún sensor emite señal)

9.3. Bloque principal

9.3.1. Resumen

El bloque principal realiza 5 operaciones: primero comprueba el valor de cada sensor, y después calcula en funciona de estos que orden enviar a los motores.

9.3.2. Descripción

El bloque principal empieza en la etiqueta `main`, La posición de memoria etiquetada como `index` contiene en sus cuatro bits inferiores que sensores tiene un objeto (p.e. una pared cerca) y se pone a 0000 (no hay objetos en ninguna dirección) antes de mirar cada sensor.

El programa que comprueba los sensores es igual para los cuatro sensores: Primero se carga `SENS_I` y `SENS_O` con los valores adecuados para ese sensor. Después se llama a la rutina `lee_sensor` que devuelve en `w` la distancia a la que encontró un objeto o `Max_dist` si no lo encontró.

Este valor se compara con `SensorNd` (siendo `N` el numero de sensor) y en caso de que el sensor encontrase algo antes de esa distancia se pone a 1 el bit correspondiente en el registro `index`.

Esta operación se repite con los cuatro sensores.

Una vez mirados los cuatro sensores, se llama a la subrutina `tabla` con `index` en `w`, esta rutina devuelve en `w` un numero con la combinación de motores que se debe encender.

Se coloca este valor en el puerto A y se vuelve a empezar el ciclo.

La subrutina tabla no requiere mayor explicación, simplemente aprovecha la instrucción `retlw` para retornar un determinado valor en función de `w`. Esta tabla de dieciséis valores contiene la forma de actuar del robot en función de los sensores, y cambiando los valores, cambiamos el comportamiento del robot.

9.4. Rutina de Lectura de los sensores

9.4.1. Resumen

Esta rutina tras comprobar que no hay eco de anteriores operaciones, emite un pulso de ultrasonidos y luego calcula el tiempo que tarda en volver el eco.

9.4.2. Descripción

Lo primero que hace esta rutina es comprobar que no se recibe ninguna señal por el sensor correspondiente, y espera a que este cese en caso contrario.

Después emite una señal de una duración cercana a medio milisegundo, exactamente $0{,}512mS$, por razones de sencillez de programación. Se programa el timer y se espera a que este de un timeout, tras lo cual se silencia el emisor de ultrasonidos.

Se reprograma el prescaler del temporizador a 1/64 de CLK/4, esto es a $64\mu S$, lo que permitirá una resolución ligeramente superior a 1cm. Programamos el timer, y activamos las interrupciones, bien por cambio en alguna entrada del puerto B, bien por desbordamiento del timer.

Ponemos el bit 0 del registro `espera` a 0, y esperamos a que este cambie (cosa que sucede en la rutina de respuesta a interrupciones), tras lo cual cargamos la distancia en `w` y retornamos.

9.5. Rutina de respuesta a las interrupciones

9.5.1. Resumen

Las interrupciones están activadas mientras se espera el eco de cada sensor.

Esta rutina comprueba si el eco es correcto, o si se ha producido un desbordamiento del timer, y actúa en consecuencia.

9.5.2. Descripción

Lo primero que se hace es guardar el estado de `status` y `w`, en unos registros temporales, luego se salta a la verdadera rutina de gestión de las interrupciones.

Comprobamos si se produjo el overflow, y en ese caso, cargamos `w` con el valor de `Max_dist` y saltamos al final de la rutina.

Si la interrupción no era por overflow, fue por un cambio en alguna entrada del puerto B, comprobamos que la entrada que nos interesa a cambiado, si no fuese así, saltaríamos a `novint`.

Si la interrupción fue valida, calculamos la distancia, para ellos recuperamos el valor del timer, eliminamos los bits que no interesan con una operación `AND` y pasamos al final de la rutina.

En el final de la rutina se activa el bit 0 de espera lo que indicara a la rutina de medida que ya obtuvimos una respuesta, se recupera el valor de `status` y `w` y se retorna.

Si causa de la interrupción no es valida, se llegaría a `novint` donde se volvería a configurar las interrupciones, se recupera el valor de `status` y `w` y se retorna activando las interrupciones.

9.6. Listado del Programa

```
;******************************************************************
;                                                                 *
; Robot autonomo controlado por ultrasonidos.                     *
;                                                                 *
; Template file assembled with MPLAB V4.00.00 and MPASM V2.20.12. *
;                                                                 *
;******************************************************************
;                                                                 *
;  Filename:     p1.asm                                           *
;  Date:         14/05/2003                                       *
;  File Version: 1.1                                              *
;                                                                 *
;  Author:       Alvaro Alea Fernandez                            *
;  Company:      Escuela de Ingenieria Tecnica Industrial de Gijon *
;  License:      GPL Version 2                                    *
;                                                                 *
;******************************************************************
;                                                                 *
;    Files required:                                              *
;                                                                 *
;******************************************************************
;                                                                 *
;    Notes:                                                       *
;                                                                 *
;******************************************************************


       list      p=16F84A     ; list directive to define processor
       #include <p16F84A.inc> ; processor specific variable definitions

       __CONFIG   _CP_OFF & _WDT_OFF & _PWRTE_ON & _XT_OSC

; '__CONFIG' directive is used to embed configuration data within .asm
; file. The lables following the directive are located in the respective
; .inc file. See respective data sheet for additional information on
; configuration word.

;***** VARIABLE DEFINITIONS
w_temp      EQU   0x0C ; variable used for context saving
status_temp EQU   0x0D ; variable used for context saving
SENS_I      EQU   0x0E ; Utilizados para leer cada sensor
SENS_O      EQU   0x0F
espera      EQU   0x10 ; utilizadas para medir distancias.
dist        EQU   0x11
index       EQU   0x12

;***** CONSTANTS DEFINITIONS
Sensor1o    EQU   0x01 ; configuracion de bits de entrada y salida de
Sensor1i    EQU   0x10 ; los sensores del puerto B
```

```
Sensor2o    EQU   0x02
Sensor2i    EQU   0x20
Sensor3o    EQU   0x04
Sensor3i    EQU   0x40
Sensor4o    EQU   0x08
Sensor4i    EQU   0x80
AA          EQU   b'0101' ; para facilitar la tabla de respuestas
VV          EQU   b'1010'
AV          EQU   b'0110'
VA          EQU   b'1001'
XA          EQU   b'0001'
AX          EQU   b'0100'
XX          EQU   b'0000'
XV          EQU   b'0010'
VX          EQU   b'1000'
Sensor1d    EQU   d'10' ; ^  distancia en cm (aprox) a la que
Sensor2d    EQU   d'10' ; <  consideramos que hay obstaculo
Sensor3d    EQU   d'10' ; >
Sensor4d    EQU   d'10' ; V
Max_dist    EQU   b'00011111' ; 32 aprox 32 cm.
Max_dist_mask EQU b'11100000' ; Valor inicial del timer.

       org 0x00
       goto inicio

       org 0x04
       movwf w_temp     ; rutina generica para conservar
       swapf STATUS,w   ; status y w
       movwf status_temp
       goto trata_int

inicio bsf STATUS,RP0    ; Configuramos el puerto a
       movlw 0x00
       movwf TRISA
       bcf STATUS,RP0    ; y apagamos los motores
       movlw 0x00
       movwf PORTA

       bsf STATUS,RP0    ; Configuramos el puerto b
       movlw 0xF0
       movwf TRISB
       bcf STATUS,RP0    ; y apagamos los sensores
       movlw 0x00
       movwf PORTB

main   clrw              ; ponemos el indice a 0
       movwf index

       movlw Sensor2i    ; leemos el 1º sensor (atras)
```

```
        movwf SENS_I
        movlw Sensor2o
        movwf SENS_O
        call lee_sensor

        sublw Sensor1d     ; miramos cual es mayor

        btfss STATUS,C     ; mayor w, lejos saltamos al siguiente
        goto sensor2

        movf index,0       ; activamos el bit del indice
        iorlw 0x01
        movwf index

sensor2 movlw Sensor3i     ; leemos el 2º sensor (delante)
        movwf SENS_I
        movlw Sensor3o
        movwf SENS_O
        call lee_sensor

        sublw Sensor2d     ; miramos cual es mayor

        btfss STATUS,C     ; mayor w, lejos saltamos al siguiente
        goto sensor3

        movf index,0       ; activamos el bit del indice
        iorlw 0x02
        movwf index


sensor3 movlw Sensor4i     ; leemos el 3º sensor (izq)
        movwf SENS_I
        movlw Sensor4o
        movwf SENS_O
        call lee_sensor

        sublw Sensor3d     ; miramos cual es mayor

        btfss STATUS,C     ; mayor w, lejos saltamos al siguiente
        goto sensor4

        movf index,0       ; activamos el bit del indice
        iorlw 0x04
        movwf index

sensor4 movlw Sensor1i     ; leemos el 4º sensor (dcha)
        movwf SENS_I
        movlw Sensor1o
        movwf SENS_O
```

```
       call lee_sensor

       sublw Sensor4d    ; miramos cual es mayor

       btfss STATUS,C    ; mayor w, lejos saltamos al siguiente
       goto miratb

       movf index,0      ; activamos el bit del indice
       iorlw 0x08
       movwf index

miratb movf index,0
       call tabla        ; la tabla indica que motores activar.
       movwf PORTA       ; activamos los motores

       goto main         ; volvemos a empezar

;*****************************************************
; FIN del programa principal, Ahora subrutinas:
;*****************************************************

tabla  addwf PCL,1
       retlw AA  ;0
       retlw XA  ;1
       retlw AX  ;2
       retlw AA  ;3

       retlw AV  ;4
       retlw VA  ;5
       retlw AV  ;6
       retlw VV  ;7

       retlw AA  ;8
       retlw XA  ;9
       retlw AX  ;10
       retlw AA  ;11

       retlw AV  ;12
       retlw VA  ;13
       retlw AV  ;14
       retlw AV  ;15

; la tabla se ha echo en funcion de lo siguiente:
; sensor 1 derecha
; sensor 2 izquierda
; sensor 3 delante
; sensor 4 detras

lee_sensor bcf STATUS,RP0 ; silenciamos los sensores
```

```
       movlw 0x00
       movwf PORTB

espera1 movf PORTB,W      ;  esperamos  a que se silecie.
       andwf SENS_I,0
       btfss STATUS,Z
       goto espera1

       movfw SENS_O        ; enviamos la señal
       movwf PORTB
                  ; esperamos 256x2us =0.512ms durante los que
                  ; hay señal
       bsf STATUS,RP0     ; banco 1
       movlw b'10000111' ; asignamos el prescaler=1/256 al timer
       movwf OPTION_REG
       bcf STATUS,RP0     ; banco 0
       movlw 0xff-0x02    ;  programamos 2 ciclos
       movwf TMR0
       movlw b'00000000' ; ponemos a 0 las int y las evitamos
       movwf INTCON
espera2 btfss INTCON,T0IF ; esperamos a que se produzca el overflow
       goto espera2       ; de T0

       movlw 0x00         ; y silenciamos la señal
       movwf PORTB

                  ; esperamos señal o timeout
       bsf STATUS,RP0     ; banco 1
       movlw b'10000101 ' ; asignamos el prescaler=1/64 al timer,
                          ; un tick=1cm aprox.
       movwf OPTION_REG
       bcf STATUS,RP0     ; banco 0
       movlw Max_dist_mask ;  ajustamos el timeout del temporizador
       movwf TMR0
       movlw b'10101000'  ; ponemos a 0 las int y permitimos por
                          ; overflow o por puerto b
       movwf INTCON
       bcf espera,0       ; esperamos la int
espera3 btfss espera,0
       goto espera3
                 ; ponemos distancia en w
       movfw dist
       return

trata_int bcf STATUS,RP0  ; banco 0
       btfss INTCON,T0IF  ; comprobamos si la INT fue por overflow
       goto nooverflow
       movlw Max_dist     ; entonces dist =128 aprox 1,28 M
       movwf dist
```

```
       goto int2
nooverflow movf PORTB,0   ; miramos si era un eco en otro sensor
                          ; o era el que interesa
       andwf SENS_I,0
       btfsc STATUS,Z     ; si era cero int equivocada, continuamos
       goto novint
       movf TMR0,0        ; calculamos la distancia.
       andlw Max_dist
       movwf dist
int2   bsf espera,0       ; se termino la espera

       swapf status_temp,w ; rutina generica de recuperacion
       movwf STATUS       ; de w y status
       swapf w_temp,f
       swapf w_temp,w
       return

novint movlw b'00101000'  ; habilitamos las int de nuevo y volvemos.
       movwf INTCON

       swapf status_temp,w ; rutina generica de recuperacion
       movwf STATUS       ; de w y status
       swapf w_temp,f
       swapf w_temp,w
       retfie

       end
```

Capítulo 10

Realización del Microrobot

10.1. Diseño y preparación

Lo primero que se desarrollo fue el sensor de ultrasonidos, debido carencias en la documentación de los fabricantes del NE555 [10], no se utilizo un oscilador astable con un duty cycle del 50 % que el fabricante propone, en su lugar se utilizo uno con un duty cycle del 51 % que el fabricante propone con un circuito diferente.

En la parte receptora del sensor de ultrasonidos, se realizo un montaje basado en un amplificador a transistores, se introdujo un circuito rectificador de media onda, para convertir la secuencia de pulsos en uno solo del ancho de la secuencia.

Este circuito tubo que ser modificado debido a las tolerancias del amplificador operacional que hacian que unos circuitos funcionasen y otros no.

Una vez claros los circuitos se pasaron a ordenador y se generaron las placas de circuito impreso utilizando el software Eagle de cadsoft, que uso gratuito (con limitaciones) y funciona bajo Windows y Linux.

Este programa permite exportar un archivo de taladros para automatizar el proceso de creación de la PCB, aunque no se utilizo esta opción.

El soporte de los sensores y de la batería se diseño con el programa de cad QCAD, con el que se imprimieron plantillas que luego se utilizarían en la realización.

Tras el diseño físico se paso a realizar la programación del Microcontrolador, se realizo en ensamblador, utilizando el entorno integrado MPLAB que incluye un editor, ensamblador y un emulador, que permitió verificar el correcto funcionamiento de cada una de las partes del programa antes de grabarlas en el microcontrolador.

10.2. Realización

Para la realización del soporte de baterías se pego la plantillas sobre la lamina de hierro y después se corto y taladro con un útil tipo dremell.

El soporte de los sensores de realizo de manera similar, mediante una plantilla sobre madera.

Se corto las varilla roscada a la medida necesitada.

Se imprimieron en acetato los dibujos de las pistas de cobre para las placas de circuito impreso, que luego se encargaron hacer, utilizando placas fotosensibles en una insoladora y atacando las pistas con cloruro férrico.

Se soldaron todos los componente, todos los circuitos integrados, utilizaron zócalos, y se procedió a calibrar los sensores de ultrasonidos con ayuda de un osciloscopio y de un generador de funciones.

Se realizaron los 4 cables con conectores que unen cada uno de los circuitos.

Se grabo el programa en el Microcontrolador y se inserto en la placa principal.

Se realizo el montaje de las diferentes partes que forman el robot, uniendo con tirafondos las partes de madera, y con tornillos de métrica 3 el resto, utilizando separadores de circuito impreso para los sensores y circuito principal.

Por ultimo se procedió a ajustar la orientación de los sensores y la plataforma sobre la base, así como los valores limites utilizados en el programa del pic.

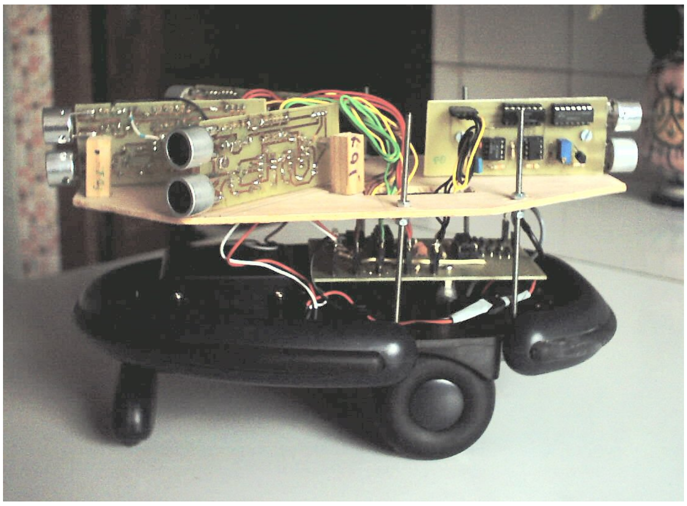

Figura 10.1: El robot una vez terminada su construcción.

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[12] Hoja de Caracteristicas 1N4007ID, 1996, Philips.

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[14] Hoja de Caracteristicas LM78XX, 1995, National Semiconductor.

[15] Hoja de Caracteristicas Motor RE-140RA, Mabuchi.

Apéndice A

Hojas de caracteristicas

Se proporcionan las siguientes hojas de caracterisiticas:
Dispositivos de la placa principal.

- Microchip PIC 16F84A
- C.I. L293E
- C.I. LM7805
- Diodo 1N4001
- Motor Mabuchi RE-140RA

Dispositivos de los sensores de ultrasonidos.

- Capsula de Ultrasonidos
- C.I. NE555
- C.I. TL081
- C.I. 7408
- C.I. 40106
- Transistor BC546
- Diodo 1N4148

PIC16F84A Data Sheet

18-pin Enhanced FLASH/EEPROM

8-bit Microcontroller

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- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
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MICROCHIP

PIC16F84A

18-pin *Enhanced* FLASH/EEPROM 8-Bit Microcontroller

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single-cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of Data RAM
- 64 bytes of Data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 Special Function Hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt-on-change
  - Data EEPROM write complete

Peripheral Features:

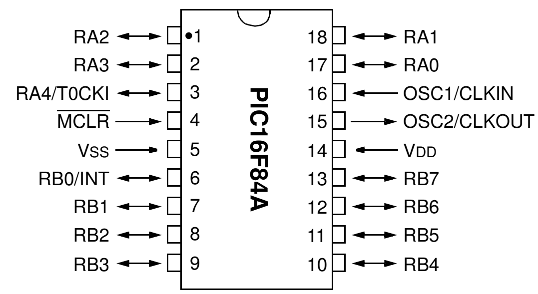
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

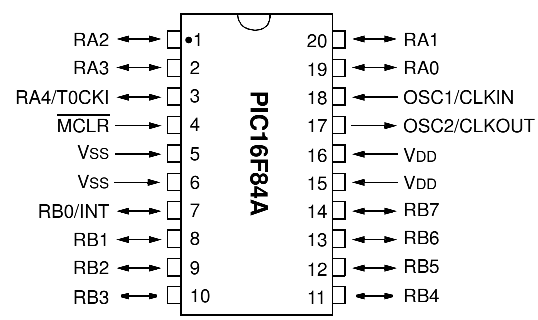
- 10,000 erase/write cycles *Enhanced* FLASH Program memory typical
- 10,000,000 typical erase/write cycles EEPROM Data memory typical
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming™ (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Code protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagrams

PDIP, SOIC



SSOP



CMOS Enhanced FLASH/EEPROM Technology:

- Low power, high speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 5.5V
  - Industrial: 2.0V to 5.5V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 0.5 µA typical standby current @ 2V

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1.0 DEVICE OVERVIEW

This document contains device specific information for the operation of the PIC16F84A device. Additional information may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F84A belongs to the mid-range family of the PICmicro® microcontroller devices. A block diagram of the device is shown in Figure 1-1.

The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16F84A BLOCK DIAGRAM

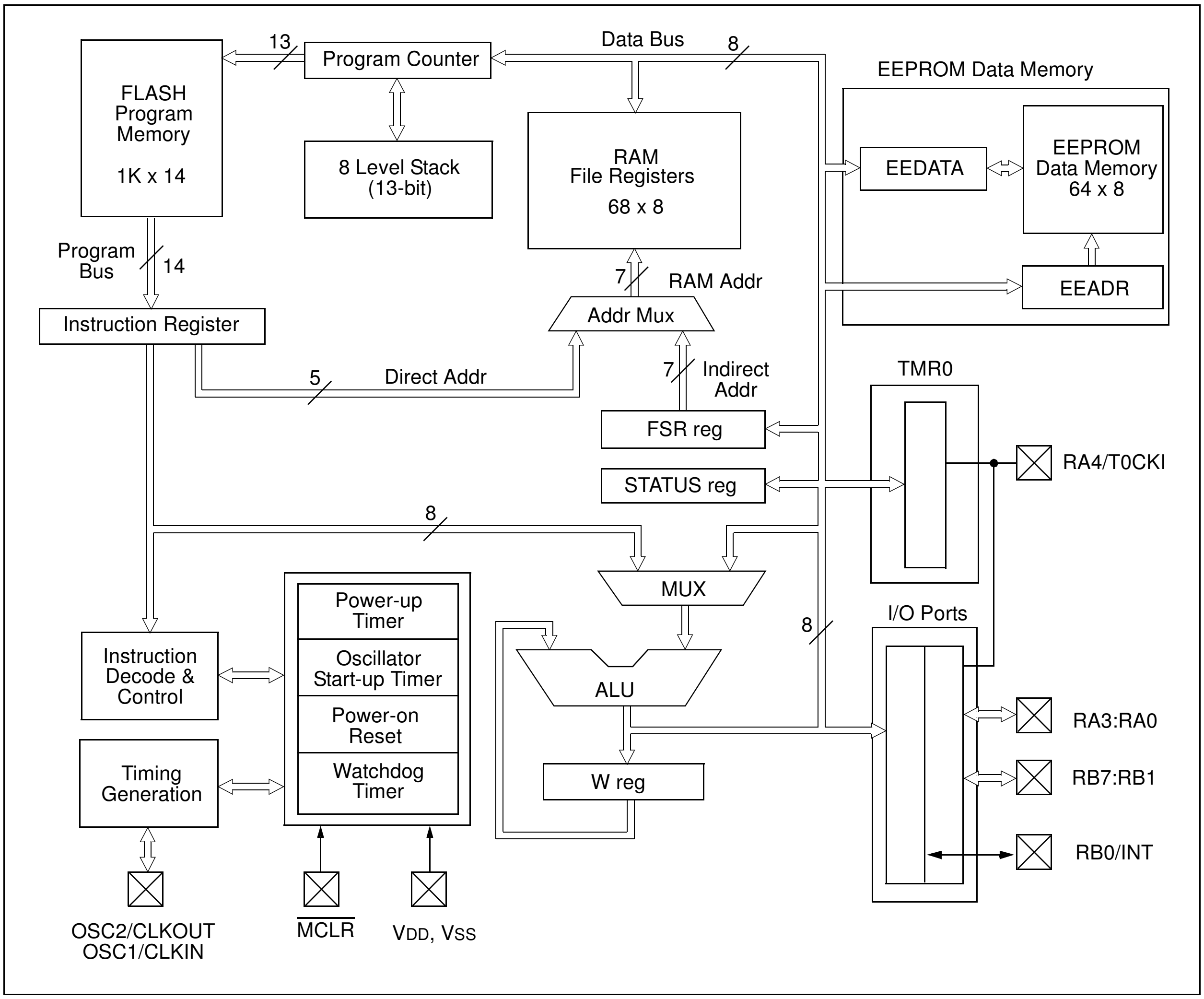


TABLE 1-1: PIC16F84A PINOUT DESCRIPTION

Pin Name	PDIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{\text{MCLR}}$	4	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt-on-change pin.
RB5	11	11	12	I/O	TTL	Interrupt-on-change pin.
RB6	12	12	13	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
VSS	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = Output I/O = Input/Output P = Power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F84A. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the “core” are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 3.0.

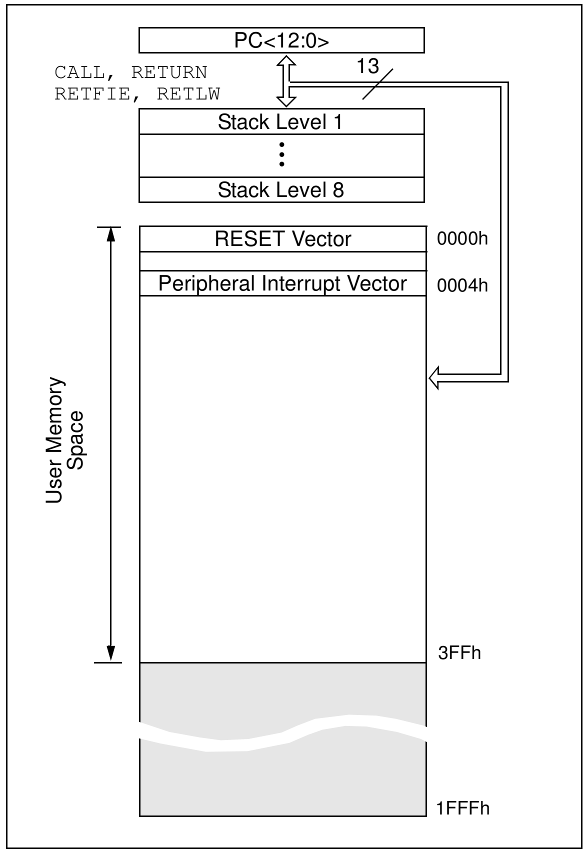
Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F84A, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 2-1). Accessing a location above the physically implemented address will cause a wraparound. For example, for locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h, the instruction will be the same.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A



2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-2 shows the data memory map organization.

Instructions `MOVWF` and `MOVF` can move values from the W register to any location in the register file (“F”), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.5). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers, implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8-bits wide and is accessed either directly or indirectly through the FSR (Section 2.5).

The GPR addresses in Bank 1 are mapped to addresses in Bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A

File Address	Bank 0	Bank 1	File Address
00h	Indirect addr.(1)	Indirect addr.(1)	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	—	—	87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2(1)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch–4Fh	68 General Purpose Registers (SRAM)	Mapped (accesses) in Bank 0	8Ch–CFh
50h–7Fh			D0h–FFh

☐ Unimplemented data memory location, read as ’0’.

Note 1: Not a physical register.

2.3 Special Function Registers

The Special Function Registers (Figure 2-2 and Table 2-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

TABLE 2-1: SPECIAL FUNCTION REGISTER FILE SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- ----	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS(2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA(4)	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB(5)	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC(1)					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- ----	11
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	16
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC(1)					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ Reset.

3: Other (non power-up) RESETS include: external RESET through $\overline{MCLR}$ and the Watchdog Timer Reset.

4: On any device RESET, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

2.3.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 7-2), because these instructions do not affect any status bit.

> **Note 1:** The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
>
> **2:** The C and DC bits operate as a $\overline{\text{borrow}}$ and digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.
>
> **3:** When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

bit 7-6 **Unimplemented:** Maintain as ‘`0`’

bit 5 **RP0**: Register Bank Select bits (used for direct addressing)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)

bit 4 **$\overline{\text{TO}}$**: Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$**: Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z**: Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{\text{borrow}}$, the polarity is reversed)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{\text{borrow}}$, the polarity is reversed)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

> **Note:** A subtraction is executed by adding the two’s complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

2.3.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note:	When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

REGISTER 2-2: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.3.3 INTCON REGISTER

The INTCON register is a readable and writable register that contains the various enable bits for all interrupt sources.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **EEIE**: EE Write Complete Interrupt Enable bit
1 = Enables the EE Write Complete interrupts
0 = Disables the EE Write Complete interrupt

bit 5 **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

2.4 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. If the program counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`. All updates to the PCH register go through the PCLATH register.

2.4.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

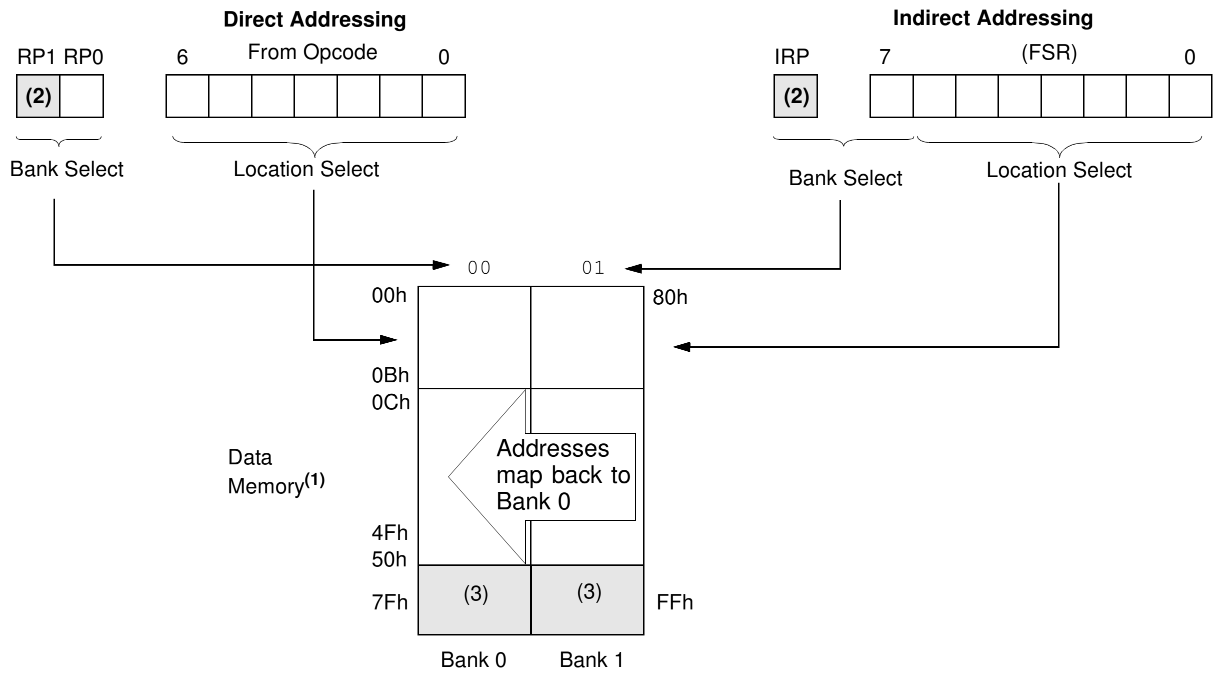
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
         :              ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-3. However, IRP is not used in the PIC16F84A.

FIGURE 2-3: DIRECT/INDIRECT ADDRESSING



Note 1: For memory map detail, see Figure 2-2.

2: Maintain as clear for upward compatibility with future products.

3: Not implemented.

3.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2 (not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F84A devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

REGISTER 3-1: EECON1 REGISTER (ADDRESS 88h)

U-0	U-0	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	EEIF	WRERR	WREN	WR	RD
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{MCLR}$ Reset or any WDT Reset during normal operation)
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the EEPROM

bit 1 **WR:** Write Control bit
1 = Initiates a write cycle. The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
0 = Does not initiate an EEPROM read

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

3.1 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore, it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-1: DATA EEPROM READ

```
BCF      STATUS, RP0  ; Bank 0
MOVLW    CONFIG_ADDR  ;
MOVWF    EEADR        ; Address to read
BSF      STATUS, RP0  ; Bank 1
BSF      EECON1, RD   ; EE Read
BCF      STATUS, RP0  ; Bank 0
MOVF     EEDATA, W    ; W = EEDATA
```

3.2 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 3-2: DATA EEPROM WRITE

```
          BSF      STATUS, RP0  ; Bank 1
          BCF      INTCON, GIE  ; Disable INTs.
          BSF      EECON1, WREN ; Enable Write
          MOVLW    55h          ;
Required  MOVWF    EECON2       ; Write 55h
Sequence  MOVLW    AAh          ;
          MOVWF    EECON2       ; Write AAh
          BSF      EECON1,WR    ; Set WR bit
                                ;   begin write
          BSF      INTCON, GIE  ; Enable INTs.
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

3.3 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 3-3) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit.

Generally, the EEPROM write failure will be a bit which was written as a '0', but reads back as a '1' (due to leakage off the bit).

EXAMPLE 3-3: WRITE VERIFY

```
      BCF   STATUS,RP0  ; Bank 0
      :                 ; Any code
      :                 ; can go here
      MOVF  EEDATA,W    ; Must be in Bank 0
      BSF   STATUS,RP0  ; Bank 1
READ
      BSF   EECON1, RD  ; YES, Read the
                        ; value written
      BCF   STATUS, RP0 ; Bank 0
                        ;
                        ; Is the value written
                        ; (in W reg) and
                        ; read (in EEDATA)
                        ; the same?
                        ;
      SUBWF EEDATA, W   ;
      BTFSS STATUS, Z   ; Is difference 0?
      GOTO  WRITE_ERR   ; NO, Write error
```

TABLE 3-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
08h	EEDATA	EEPROM Data Register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM Address Register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM Control Register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends upon condition.
Shaded cells are not used by data EEPROM.

4.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual (DS33023).

4.1 PORTA and TRISA Registers

PORTA is a 5-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as inputs and read as '0'.

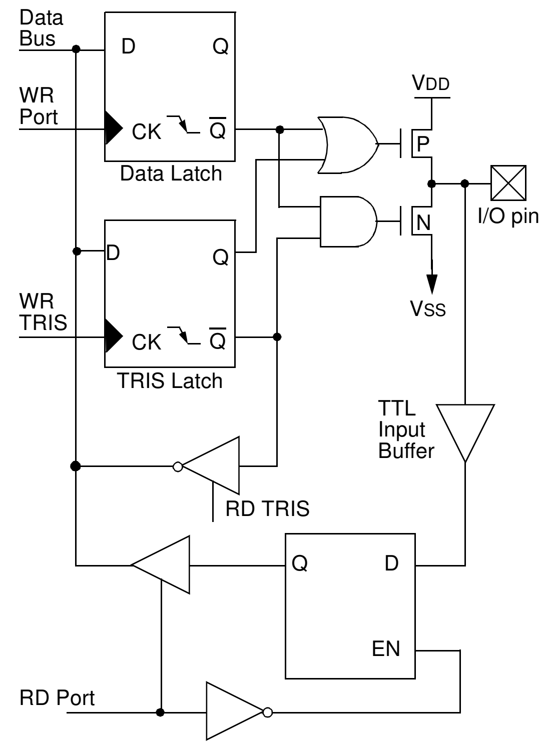
Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read. This value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

EXAMPLE 4-1: INITIALIZING PORTA

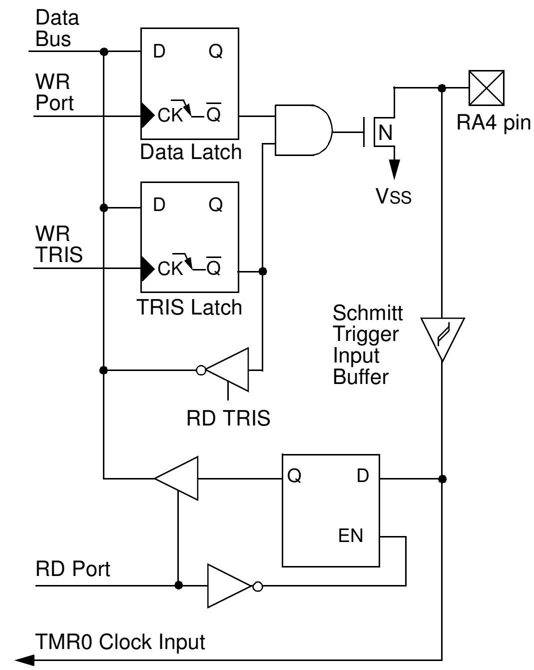
```
BCF     STATUS, RP0 ;
CLRF    PORTA       ; Initialize PORTA by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA4 as output
                    ; TRISA<7:5> are always
                    ; read as '0'.
```

FIGURE 4-1: BLOCK DIAGRAM OF PINS RA3:RA0



Note: I/O pins have protection diodes to V_{DD} and V_{SS}.

FIGURE 4-2: BLOCK DIAGRAM OF PIN RA4



Note: I/O pins have protection diodes to V_{DD} and V_{SS}.

TABLE 4-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	`---x xxxx`	`---u uuuu`
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	`---1 1111`	`---1 1111`

Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented, read as '0'. Shaded cells are unimplemented, read as '0'.

4.2 PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

EXAMPLE 4-2: INITIALIZING PORTB

```
BCF     STATUS, RP0 ;
CLRF    PORTB       ; Initialize PORTB by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

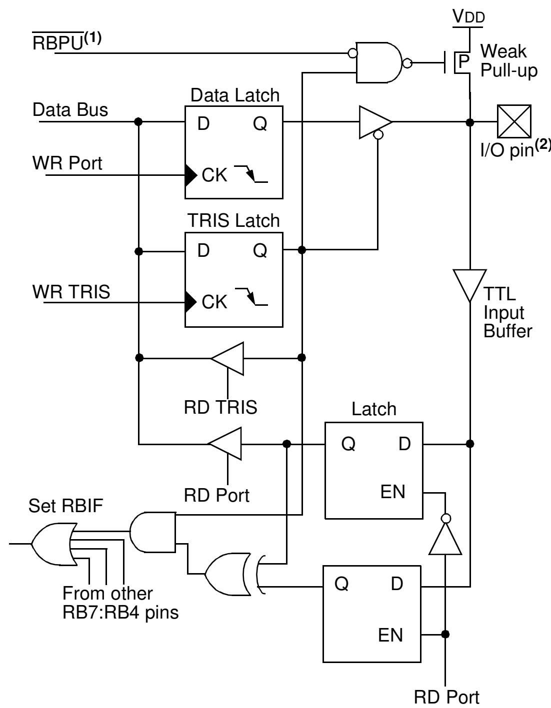
a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

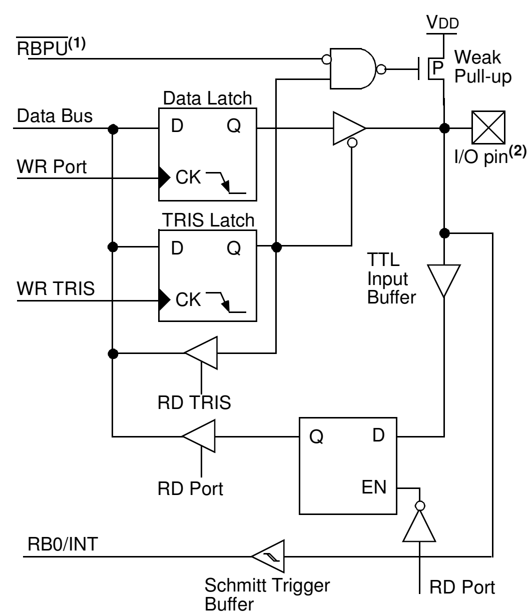
FIGURE 4-3: BLOCK DIAGRAM OF PINS RB7:RB4



Note 1: TRISB = '1' enables weak pull-up (if $\overline{\text{RBPU}}$ = '0' in the OPTION_REG register).

2: I/O pins have diode protection to VDD and VSS.

FIGURE 4-4: BLOCK DIAGRAM OF PINS RB3:RB0



Note 1: TRISB = '1' enables weak pull-up (if $\overline{\text{RBPU}}$ = '0' in the OPTION_REG register).

2: I/O pins have diode protection to VDD and VSS.

TABLE 4-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt-on-overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

5.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

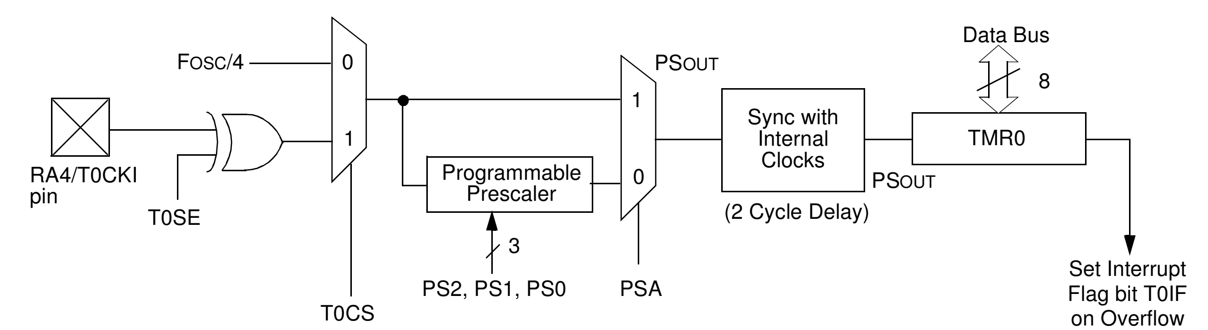
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

5.2.1 SWITCHING PRESCALER ASSIGNMENT

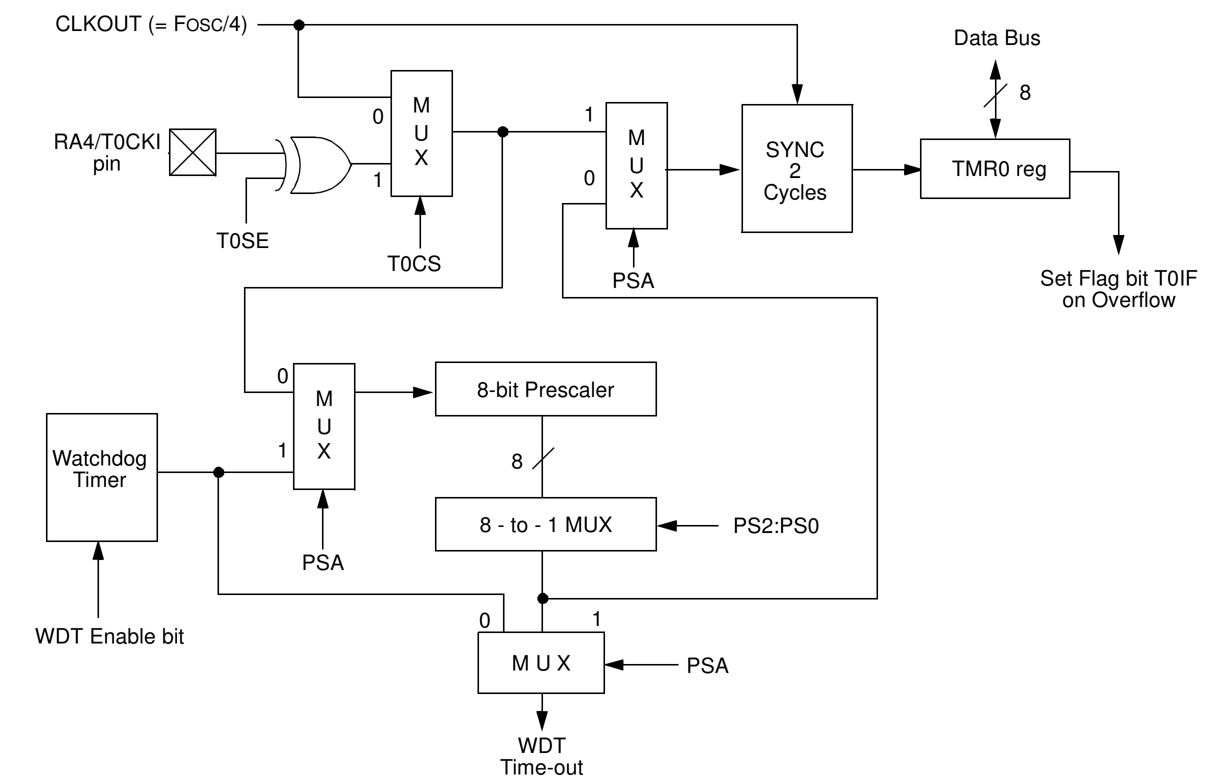
The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution).

> **Note:** To avoid an unintended device RESET, a specific instruction sequence (shown in the PICmicro™ Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

5.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut-off during SLEEP.

FIGURE 5-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION_REG<5:0>).

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

6.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F84A has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC Selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code Protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F84A has a Watchdog Timer which can be shut-off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

Additional information on special features is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

6.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

REGISTER 6-1: PIC16F84A CONFIGURATION WORD

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	F0SC1	F0SC0
bit13													bit0

bit 13-4 **CP:** Code Protection bit
1 = Code protection disabled
0 = All program memory is code protected

bit 3 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = Power-up Timer is disabled
0 = Power-up Timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

6.2 Oscillator Configurations

6.2.1 OSCILLATOR TYPES

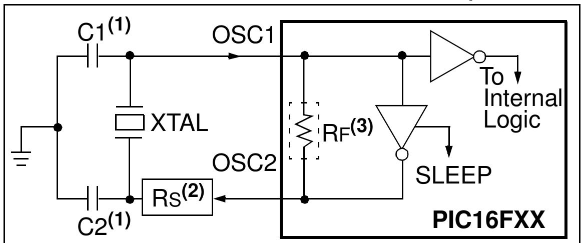
The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

6.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP, or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 6-1).

FIGURE 6-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 6-1 for recommended values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 6-2).

FIGURE 6-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

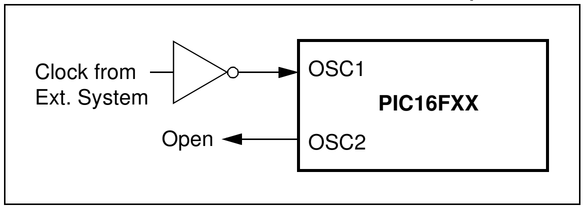


TABLE 6-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:

Mode	Freq	OSC1/C1	OSC2/C2
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested in this table. Higher capacitance increases the stability of the oscillator, but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.

Note: When using resonators with frequencies above 3.5 MHz, the use of HS mode rather than XT mode, is recommended. HS mode may be used at any VDD for which the controller is rated.

TABLE 6-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

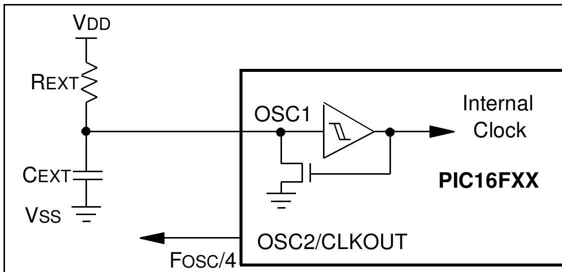
Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz 200 kHz	68 - 100 pF 15 - 33 pF	68 - 100 pF 15 - 33 pF
XT	100 kHz 2 MHz 4 MHz	100 - 150 pF 15 - 33 pF 15 - 33 pF	100 - 150 pF 15 - 33 pF 15 - 33 pF
HS	4 MHz 20 MHz	15 - 33 pF 15 - 33 pF	15 - 33 pF 15 - 33 pF

Note: Higher capacitance increases the stability of the oscillator, but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode, as well as XT mode, to avoid over-driving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

6.2.3 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) values, capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low CEXT values. The user needs to take into account variation, due to tolerance of the external R and C components. Figure 6-3 shows how an R/C combination is connected to the PIC16F84A.

FIGURE 6-3: RC OSCILLATOR MODE



Recommended values: 5 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20pF

6.3 RESET

The PIC16F84A differentiates between various kinds of RESET:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ during normal operation
- $\overline{\text{MCLR}}$ during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

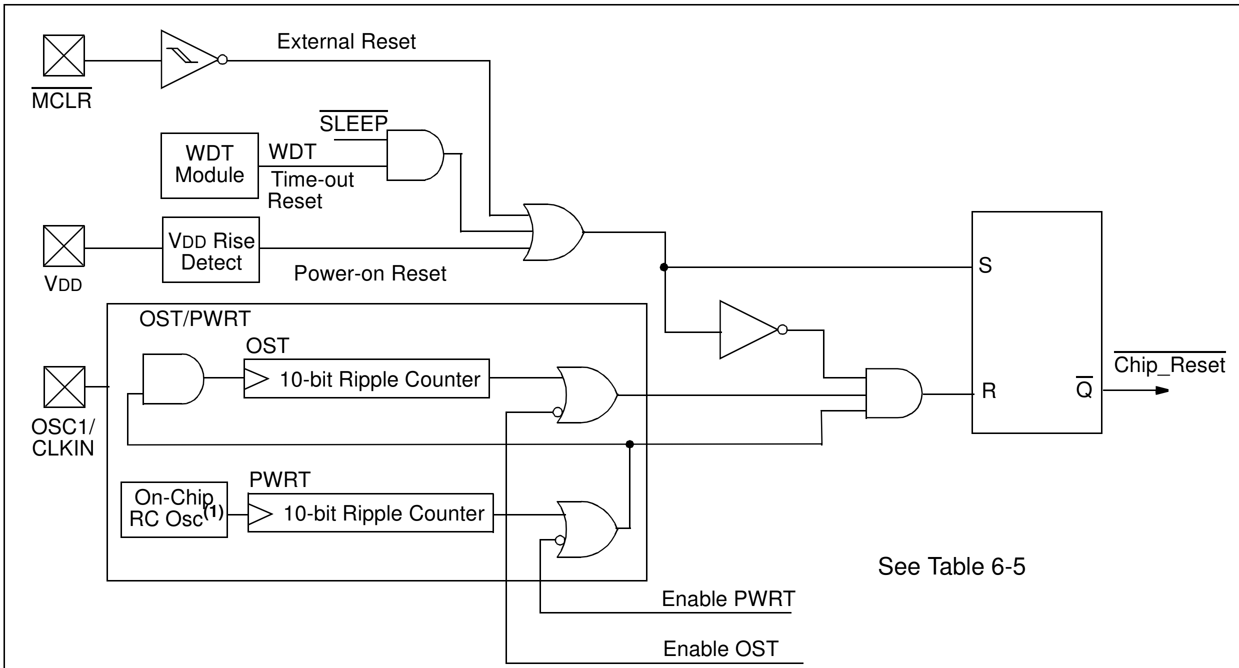
Figure 6-4 shows a simplified block diagram of the On-Chip RESET Circuit. The $\overline{\text{MCLR}}$ Reset path has a noise filter to ignore small pulses. The electrical specifications state the pulse width requirements for the $\overline{\text{MCLR}}$ pin.

Some registers are not affected in any RESET condition; their status is unknown on a POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on POR, $\overline{\text{MCLR}}$ or WDT Reset during normal operation and on $\overline{\text{MCLR}}$ during SLEEP. They are not affected by a WDT Reset during SLEEP, since this RESET is viewed as the resumption of normal operation.

Table 6-3 gives a description of RESET conditions for the program counter (PC) and the STATUS register. Table 6-4 gives a full description of RESET states for all registers.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different RESET situations (Section 6.7). These bits are used in software to determine the nature of the RESET.

FIGURE 6-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.
2: See Table 6-5.

TABLE 6-3: RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
$\overline{\text{MCLR}}$ during normal operation	000h	000u uuuu
$\overline{\text{MCLR}}$ during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu

Legend: u = unchanged, x = unknown
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 6-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1(2)
STATUS	03h	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA (4)	05h	---x xxxx	---u uuuu	---u uuuu
PORTB (5)	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu(1)
INDF	80h	---- ----	---- ----	---- ----
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000 0000	0000 0000	PC + 1(2)
STATUS	83h	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu(1)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: Table 6-3 lists the RESET value for each specific condition.

4: On any device RESET, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

6.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*."

The POR circuit does not produce an internal RESET when VDD declines.

6.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figures 6-6 through 6-9). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level (possible exception shown in Figure 6-9).

A configuration bit, $\overline{\text{PWRTE}}$, can enable/disable the PWRT. See Register 6-1 for the operation of the $\overline{\text{PWRTE}}$ bit for a particular device.

The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

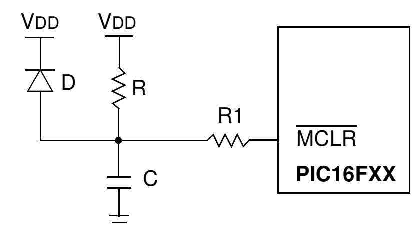
6.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 6-6, Figure 6-7, Figure 6-8 and Figure 6-9). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case (Figure 6-9), an external Power-on Reset circuit may be necessary (Figure 6-5).

FIGURE 6-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if VDD power-up rate is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{\text{MCLR}}$ pin is 5 µA). A larger voltage drop will degrade VIH level on the $\overline{\text{MCLR}}$ pin.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{\text{MCLR}}$ from external capacitor C, in the event of a $\overline{\text{MCLR}}$ pin breakdown due to ESD or EOS.

FIGURE 6-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 1

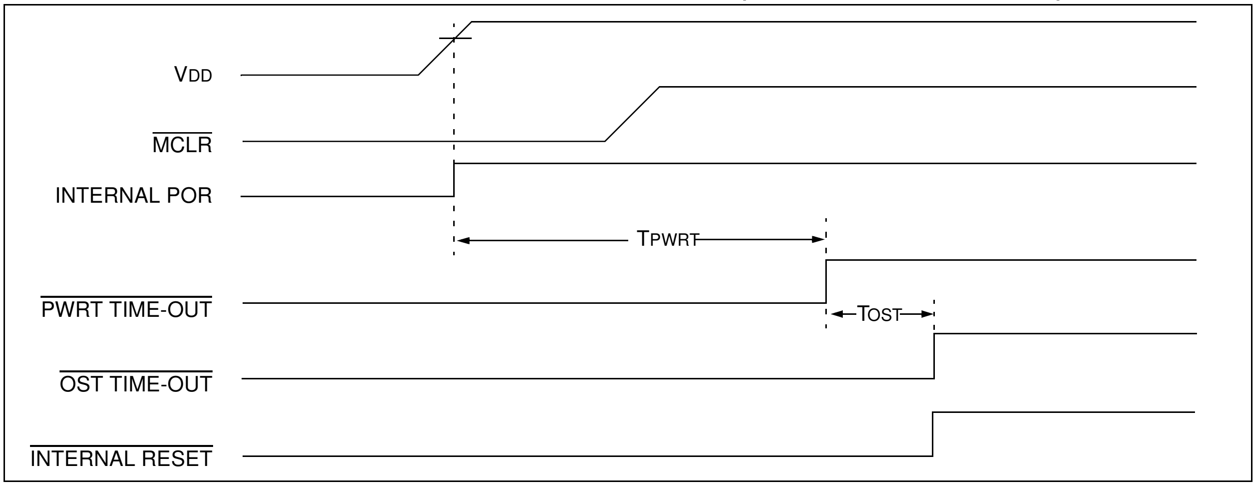


FIGURE 6-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 2

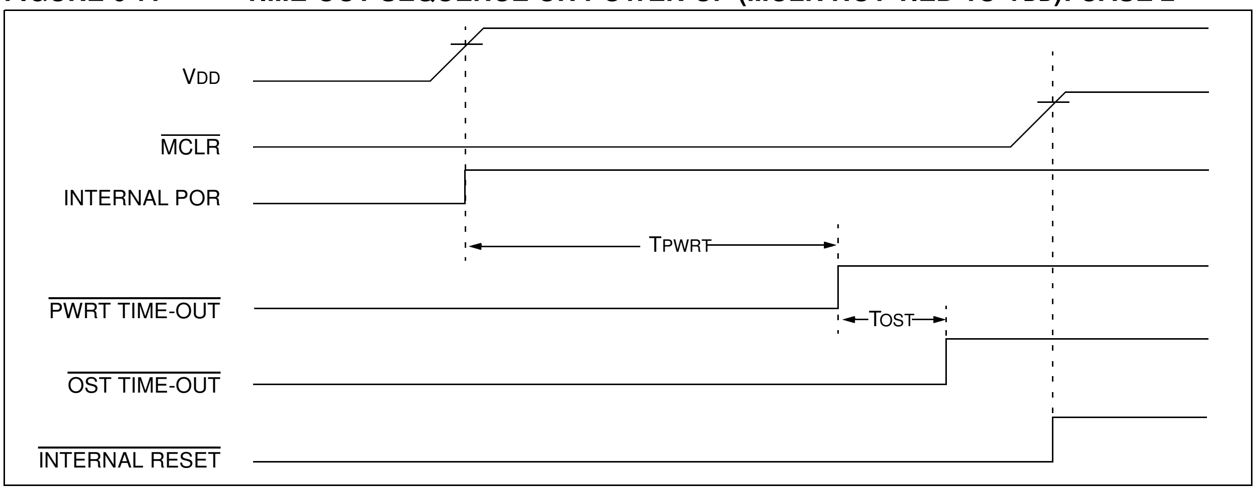


FIGURE 6-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

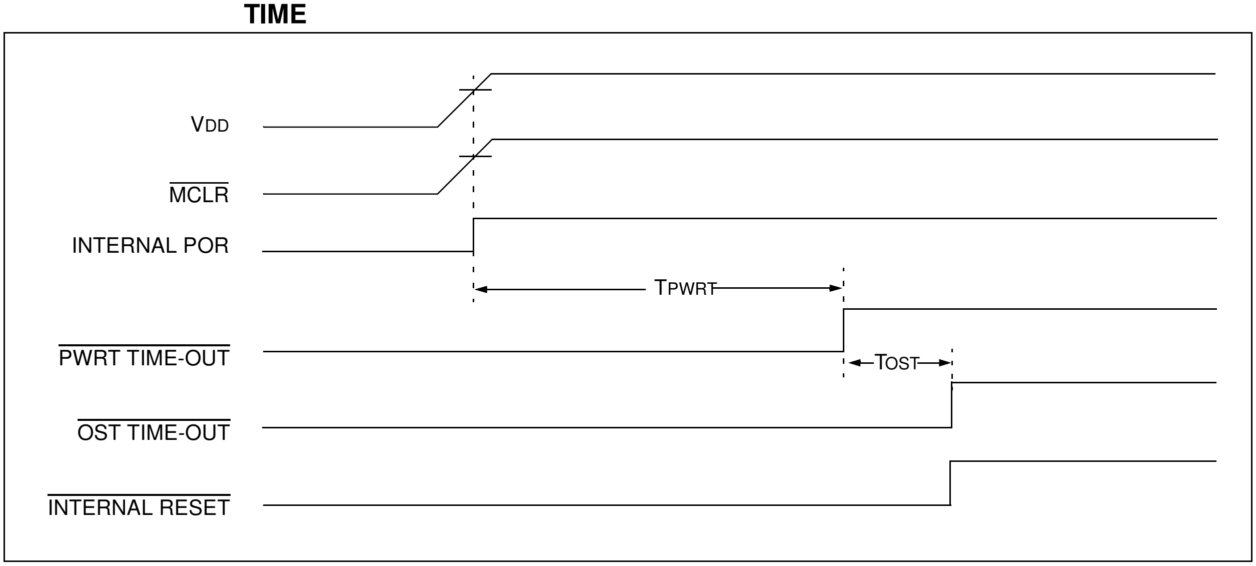
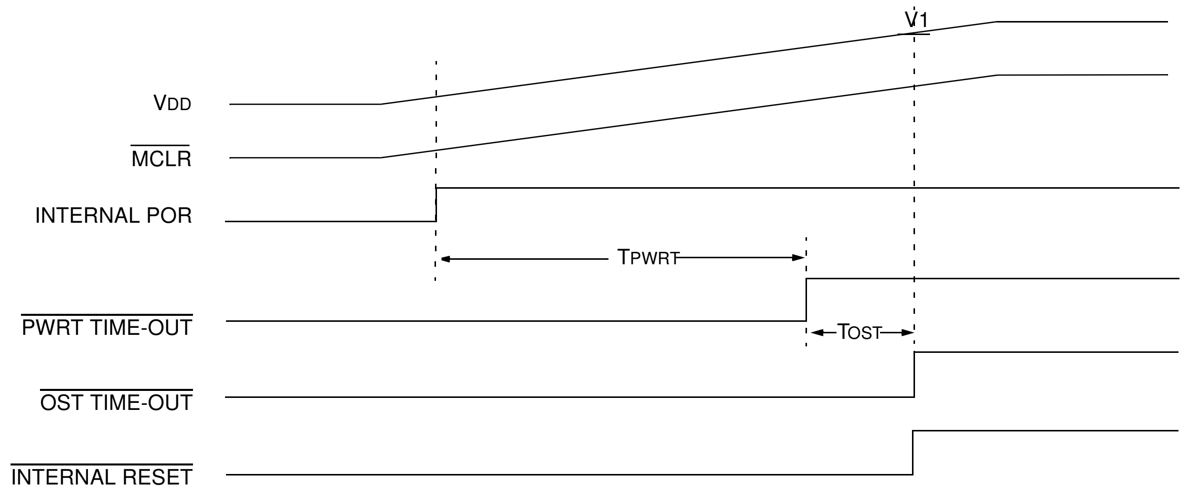


FIGURE 6-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



When V_{DD} rises very slowly, it is possible that the T_{PWRT} time-out and T_{OST} time-out will expire before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, $V1 \geq V_{DD}$ min.

6.7 Time-out Sequence and Power-down Status Bits ($\overline{TO}$/$\overline{PD}$)

On power-up (Figures 6-6 through 6-9), the time-out sequence is as follows:

1. PWRT time-out is invoked after a POR has expired.
2. Then, the OST is activated.

The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 6-5: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + $1024T_{OSC}$	$1024T_{OSC}$	$1024T_{OSC}$
RC	72 ms	—	—

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high, execution will begin immediately (Figure 6-6). This is useful for testing purposes or to synchronize more than one PIC16F84A device when operating in parallel.

Table 6-6 shows the significance of the $\overline{TO}$ and $\overline{PD}$ bits. Table 6-3 lists the RESET conditions for some special registers, while Table 6-4 lists the RESET conditions for all the registers.

TABLE 6-6: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{TO}$	$\overline{PD}$	Condition
1	1	Power-on Reset
0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	$\overline{MCLR}$ during normal operation
1	0	$\overline{MCLR}$ during SLEEP or interrupt wake-up from SLEEP

6.8 Interrupts

The PIC16F84A has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on RESET.

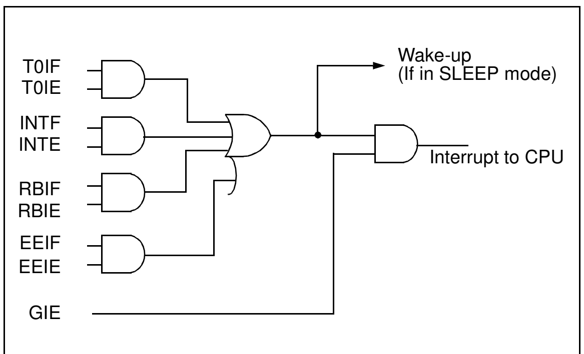
The "return from interrupt" instruction, `RETFIE`, exits interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for both one and two cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note:	Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 6-10: INTERRUPT LOGIC



6.8.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION_REG<6>) is set, or falling if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 6.11) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

6.8.2 TMR0 INTERRUPT

An overflow (FFh $\rightarrow$ 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 5.0).

6.8.3 PORTB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 4.2).

Note:	For a change on the I/O pin to be recognized, the pulse width must be at least TCY wide.

6.8.4 DATA EEPROM INTERRUPT

At the completion of a data EEPROM write cycle, flag bit EEIF (EECON1<4>) will be set. The interrupt can be enabled/disabled by setting/clearing enable bit EEIE (INTCON<6>) (Section 3.0).

6.9 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

The code in Example 6-1 stores and restores the STATUS and W register's values. The user defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 6-1 does the following:

a) Stores the W register.
b) Stores the STATUS register in STATUS_TEMP.
c) Executes the Interrupt Service Routine code.
d) Restores the STATUS (and bank select bit) register.
e) Restores the W register.

EXAMPLE 6-1: SAVING STATUS AND W REGISTERS IN RAM

```
PUSH    MOVWF   W_TEMP              ; Copy W to TEMP register,
        SWAPF   STATUS,     W       ; Swap status to be saved into W
        MOVWF   STATUS_TEMP         ; Save status to STATUS_TEMP register
ISR     :                           :
        :                           ; Interrupt Service Routine
        :                           ; should configure Bank as required
        :                           ;
POP     SWAPF   STATUS_TEMP,W       ; Swap nibbles in STATUS_TEMP register
                                    ; and place result into W
        MOVWF   STATUS              ; Move W into STATUS register
                                    ; (sets bank to original state)
        SWAPF   W_TEMP,     F       ; Swap nibbles in W_TEMP and place result in W_TEMP
        SWAPF   W_TEMP,     W       ; Swap nibbles in W_TEMP and place result into W
```

6.10 Watchdog Timer (WDT)

The Watchdog Timer is a free running On-Chip RC Oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 6.1).

6.10.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION_REG register. Thus, time-out periods up to 2.3 seconds can be realized.

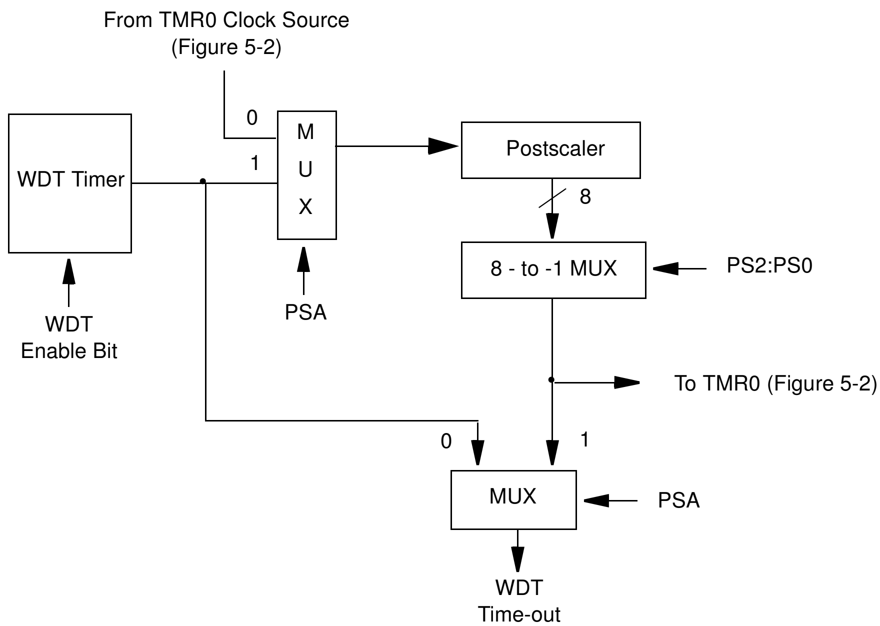
The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

6.10.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (V_{DD} = Min., Temperature = Max., Max. WDT Prescaler), it may take several seconds before a WDT time-out occurs.

FIGURE 6-11: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS2:PS0 are bits in the OPTION_REG register.

TABLE 6-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
2007h	Config. bits	**(2)**	**(2)**	**(2)**	**(2)**	$\overline{\text{PWRTE}}$(1)	WDTE	FOSC1	FOSC0	**(2)**	
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.
Note 1: See Register 6-1 for operation of the $\overline{\text{PWRTE}}$ bit.
2: See Register 6-1 and Section 6.12 for operation of the code and data protection bits.

6.11 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (wake-up from SLEEP).

6.11.1 SLEEP

The Power-down mode is entered by executing the `SLEEP` instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the PD bit (STATUS<3>) is cleared, the TO bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either V_{DD} or V_{SS}, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at V_{DD} or V_{SS}. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (V_{IHMC}).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR pin low.

6.11.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

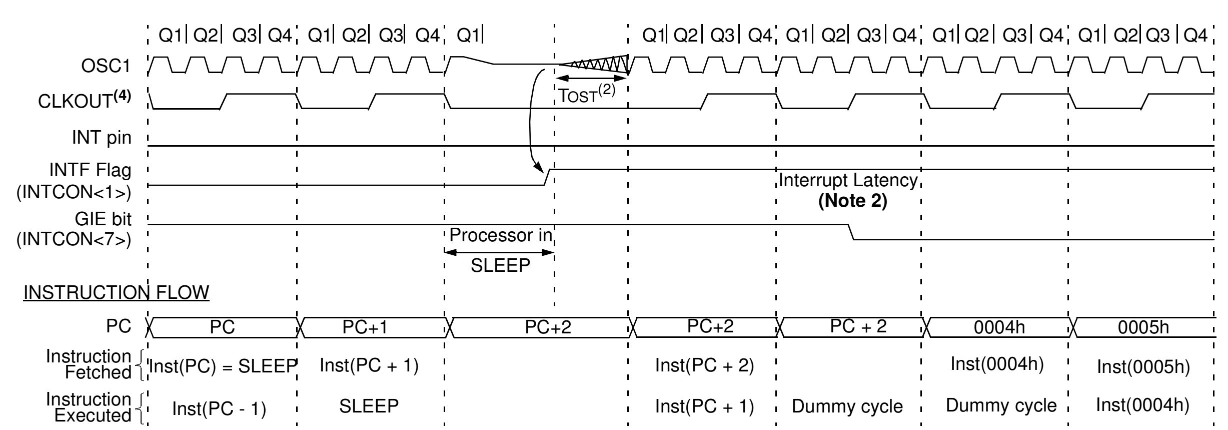
1. External RESET input on MCLR pin.
2. WDT wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event (MCLR Reset) will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits can be used to determine the cause of a device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT time-out occurred (and caused wake-up).

While the `SLEEP` instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

FIGURE 6-12: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS, or LP oscillator mode assumed.
2: T_{OST} = $1024T_{OSC}$ (drawing not to scale). This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

6.11.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from SLEEP. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the WDT is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

6.12 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

6.13 ID Locations

Four memory locations (2000h - 2004h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the four Least Significant bits of ID location are usable.

6.14 In-Circuit Serial Programming

PIC16F84A microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

For complete details of Serial Programming, please refer to the In-Circuit Serial Programming™ (ICSP™) Guide, (DS30277).

NOTES:

7.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word, divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 7-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 7-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 7-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Table 7-2 lists the instructions recognized by the MPASM™ Assembler.

Figure 7-1 shows the general formats that the instructions can have.

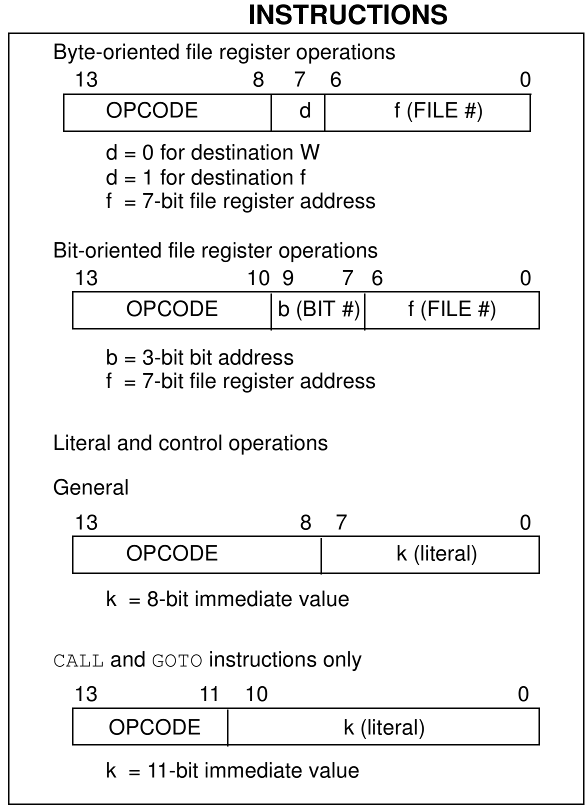
> **Note:** To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 7-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

> **Note:** Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

7.1 Instruction Descriptions

ADDLW	**Add Literal and W**
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal ’k’ and the result is placed in the W register.

ADDWF	**Add W and f**
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow$ (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register ’f’. If ’d’ is 0, the result is stored in the W register. If ’d’ is 1, the result is stored back in register ’f’.

ANDLW	**AND Literal with W**
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of W register are AND’ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	**AND W with f**
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	**Bit Clear f**
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 $\rightarrow$ (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	**Bit Set f**
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 $\rightarrow$ (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSS	**Bit Test f, Skip if Set**
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a `NOP` is executed instead, making this a $2T_{CY}$ instruction.

BTFSC — Bit Test, Skip if Clear

Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a `NOP` is executed instead, making this a 2TCY instruction.

CALL — Call Subroutine

Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1 → TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

CLRF — Clear f

Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW — Clear W

Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT — Clear Watchdog Timer

Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF — Complement f

Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

DECF — Decrement f

Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a `NOP` is executed instead, making it a 2TCY instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	0 ≤ k ≤ 2047
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	`GOTO` is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. `GOTO` is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a `NOP` is executed instead, making it a 2TCY instruction.

IORLW	Inclusive OR Literal with W
Syntax:	[*label*] IORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None
Description:	The eight-bit literal ’k’ is loaded into W register. The don’t cares will assemble as 0’s.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

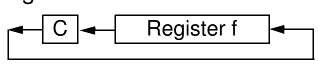
NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS $\rightarrow$ PC, 1 $\rightarrow$ GIE
Status Affected:	None

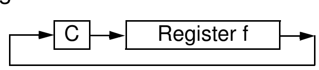
RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	k $\rightarrow$ (W); TOS $\rightarrow$ PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS $\rightarrow$ PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register ’f’ are rotated one bit to the left through the Carry Flag. If ’d’ is 0, the result is placed in the W register. If ’d’ is 1, the result is stored back in register ’f’.



RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register ’f’ are rotated one bit to the right through the Carry Flag. If ’d’ is 0, the result is placed in the W register. If ’d’ is 1, the result is placed back in register ’f’.



SLEEP	
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

SUBLW	Subtract W from Literal
Syntax:	[*label*] SUBLW k
Operands:	$0 \leq k \leq 255$
Operation:	k - (W) → (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2’s complement method) from the eight-bit literal 'k'. The result is placed in the W register.

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) - (W) → (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2’s complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

XORLW	Exclusive OR Literal with W
Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

8.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

8.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

8.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PICmicro MCU's.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

8.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

8.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

8.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

8.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows® environment were chosen to best make these features available to you, the end user.

8.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

8.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PICmicro MCUs and can be used to develop for this and other PICmicro microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

8.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PICmicro devices. It can also set code protection in this mode.

8.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PICmicro devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

8.11 PICDEM 1 Low Cost PICmicro Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

8.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I2CTM bus and separate headers for connection to an LCD module and a keypad.

8.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

8.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

8.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

TABLE 8-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 C Compiler												✓	✓						
	MPLAB® C18 C Compiler														✓	✓				
	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*			✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board			✓		✓		✓†		✓			✓							
	PICDEM™ 2 Demonstration Board				✓†			✓†							✓	✓				
	PICDEM™ 3 Demonstration Board											✓								
	PICDEM™ 14A Demonstration Board		✓																	
	PICDEM™ 17 Demonstration Board													✓						
	KEELOQ® Evaluation Kit																	✓		
	KEELOQ® Transponder Kit																	✓		
	microID™ Programmer's Kit																		✓	
	125 kHz microID™ Developer's Kit																		✓	
	125 kHz Anticollision microID™ Developer's Kit																		✓	
	13.56 MHz Anticollision microID™ Developer's Kit																		✓	
	MCP2510 CAN Developer's Kit																			✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.
** Contact Microchip Technology Inc. for availability date.
† Development tool is available on select devices.

NOTES:

9.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD}, $\overline{MCLR}$, and RA4)	-0.3V to (V_{DD} + 0.3V)
Voltage on V_{DD} with respect to V_{SS}	-0.3 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (1)	-0.3 to +14V
Voltage on RA4 with respect to V_{SS}	-0.3 to +8.5V
Total power dissipation (2)	800 mW
Maximum current out of V_{SS} pin	150 mA
Maximum current into V_{DD} pin	100 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA	50 mA
Maximum current sunk by PORTB	150 mA
Maximum current sourced by PORTB	100 mA

Note 1: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

2: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 9-1: PIC16F84A-20 VOLTAGE-FREQUENCY GRAPH

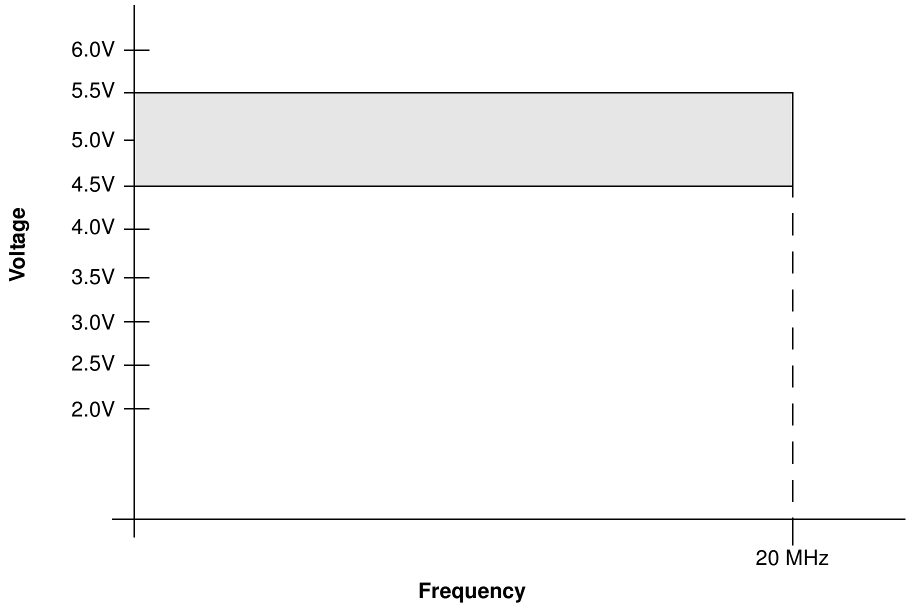
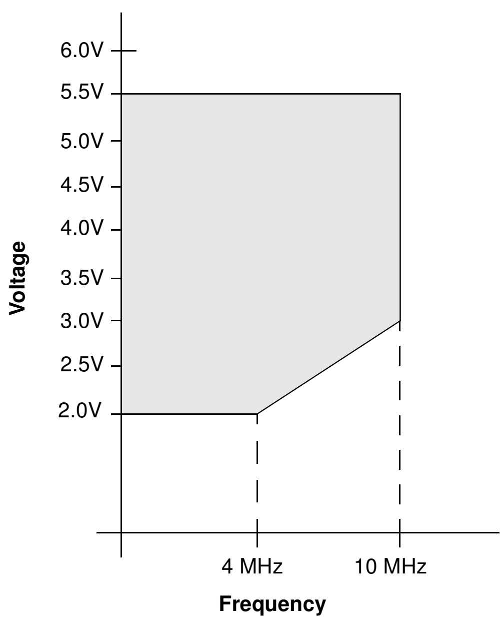


FIGURE 9-2: PIC16LF84A-04 VOLTAGE-FREQUENCY GRAPH

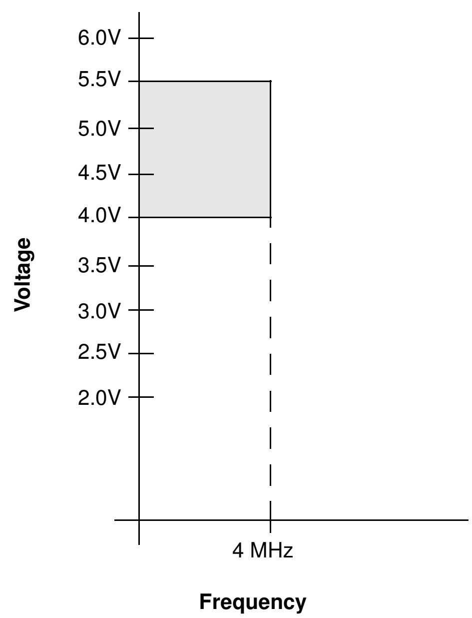


FMAX = (6.0 MHz/V) (VDDAPPMIN - 2.0V) + 4 MHz

Note 1: VDDAPPMIN is the minimum voltage of the PICmicro® device in the application.

2: FMAX has a maximum frequency of 10 MHz.

FIGURE 9-3: PIC16F84A-04 VOLTAGE-FREQUENCY GRAPH



9.1 DC Characteristics

PIC16LF84A-04 (Commercial, Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial); -40°C ≤ TA ≤ +85°C (industrial); -40°C ≤ TA ≤ +125°C (extended)				
PIC16F84A-04 (Commercial, Industrial, Extended) **PIC16F84A-20** (Commercial, Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C (commercial); -40°C ≤ TA ≤ +85°C (industrial); -40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		16LF84A	2.0	—	5.5	V	XT, RC, and LP osc configuration
D001 D001A		16F84A	4.0 4.5	— —	5.5 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002	VDR	**RAM Data Retention Voltage (Note 1)**	1.5	—	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	Vss	—	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	
	IDD	**Supply Current (Note 2)**					
D010		16LF84A	—	1	4	mA	RC and XT osc configuration **(Note 4)** FOSC = 2.0 MHz, VDD = 5.5V
D010		16F84A	—	1.8	4.5	mA	RC and XT osc configuration **(Note 4)** FOSC = 4.0 MHz, VDD = 5.5V
D010A			—	3	10	mA	RC and XT osc configuration **(Note 4)** FOSC = 4.0 MHz, VDD = 5.5V (During FLASH programming)
D013			—	10	20	mA	HS osc configuration (PIC16F84A-20) FOSC = 20 MHz, VDD = 5.5V
D014		16LF84A	—	15	45	μA	LP osc configuration FOSC = 32 kHz, VDD = 2.0V, WDT disabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NR Not rated for operation.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD,
T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula IR = VDD/2REXT (mA) with REXT in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

9.1 DC Characteristics (Continued)

PIC16LF84A-04 (Commercial, Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ T_A ≤ +70°C (commercial) -40°C ≤ T_A ≤ +85°C (industrial) -40°C ≤ T_A ≤ +125°C (extended)
PIC16F84A-04 (Commercial, Industrial, Extended) **PIC16F84A-20** (Commercial, Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ T_A ≤ +70°C (commercial) -40°C ≤ T_A ≤ +85°C (industrial) -40°C ≤ T_A ≤ +125°C (extended)

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	I_{PD}	**Power-down Current (Note 3)**					
D020		16LF84A					
D020		16F84A-20 16F84A-04					
D021A		16LF84A	—	0.4	1.0	μA	V_{DD} = 2.0V, WDT disabled, industrial
D021A		16F84A-20 16F84A-04	— —	1.5 1.0	3.5 3.0	μA μA	V_{DD} = 4.5V, WDT disabled, industrial V_{DD} = 4.0V, WDT disabled, industrial
D021B		16F84A-20 16F84A-04	— —	1.5 1.0	5.5 5.0	μA μA	V_{DD} = 4.5V, WDT disabled, extended V_{DD} = 4.0V, WDT disabled, extended
		Module Differential Current (Note 5)					
D022	ΔI_{WDT}	Watchdog Timer	— — — — —	.20 3.5 3.5 4.8 4.8	16 20 28 25 30	μA μA μA μA μA	V_{DD} = 2.0V, Industrial, Commercial V_{DD} = 4.0V, Commercial V_{DD} = 4.0V, Industrial, Extended V_{DD} = 4.5V, Commercial V_{DD} = 4.5V, Industrial, Extended

Legend: Rows with standard voltage device data only are shaded for improved readability.
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
NR Not rated for operation.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD},
T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

4: For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} measurement.

9.2 DC Characteristics: PIC16F84A-04 (Commercial, Industrial) PIC16F84A-20 (Commercial, Industrial) PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC specifications (Section 9.1)				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	VSS	—	0.8	V	4.5V ≤ VDD ≤ 5.5V **(Note 4)**
D030A			VSS	—	0.16VDD	V	Entire range **(Note 4)**
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	Entire range
D032		$\overline{\text{MCLR}}$, RA4/T0CKI	VSS	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)	VSS	—	0.3VDD	V	**(Note 1)**
D034		OSC1 (RC mode)	VSS	—	0.1VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V **(Note 4)**
D040A			0.25VDD+0.8	—	VDD	V	Entire range **(Note 4)**
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD		Entire range
D042		$\overline{\text{MCLR}}$,	0.8 VDD	—	VDD	V	
D042A		RA4/T0CKI	0.8 VDD	—	8.5	V	
D043		OSC1 (XT, HS and LP modes)	0.8 VDD	—	VDD	V	**(Note 1)**
D043A		OSC1 (RC mode)	0.9 VDD		VDD	V	
D050	VHYS	**Hysteresis of Schmitt Trigger Inputs**	—	0.1	—	V	
D070	IPURB	**PORTB Weak Pull-up Current**	50	250	400	μA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current (Notes 2, 3)**					
D060		I/O ports	—	—	±1	μA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		$\overline{\text{MCLR}}$, RA4/T0CKI	—	—	±5	μA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may choose the better of the two specs.

9.2 DC Characteristics: PIC16F84A-04 (Commercial, Industrial) PIC16F84A-20 (Commercial, Industrial) PIC16LF84A-04 (Commercial, Industrial) (Continued)

DC Characteristics **All Pins Except Power Supply Pins**			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ T_A ≤ +70°C (commercial) -40°C ≤ T_A ≤ +85°C (industrial) Operating voltage V_{DD} range as described in DC specifications (Section 9.1)				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	V_{OL}	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V
D083		OSC2/CLKOUT	—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, (RC mode only)
	V_{OH}	**Output High Voltage**					
D090		I/O ports **(Note 3)**	V_{DD}-0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V
D092		OSC2/CLKOUT **(Note 3)**	V_{DD}-0.7	—	—	V	I_{OH} = -1.3 mA, V_{DD} = 4.5V (RC mode only)
	V_{OD}	**Open Drain High Voltage**					
D150		RA4 pin	—	—	8.5	V	
		Capacitive Loading Specs on Output Pins					
D100	C_{OSC2}	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	C_{IO}	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
		Data EEPROM Memory					
D120	E_D	Endurance	1M	10M	—	E/W	25°C at 5V
D121	V_{DRW}	V_{DD} for read/write	V_{MIN}	—	5.5	V	V_{MIN} = Minimum operating voltage
D122	T_{DEW}	Erase/Write cycle time	—	4	8	ms	
		Program FLASH Memory					
D130	E_P	Endurance	1000	10K	—	E/W	
D131	V_{PR}	V_{DD} for read	V_{MIN}	—	5.5	V	V_{MIN} = Minimum operating voltage
D132	V_{PEW}	V_{DD} for erase/write	4.5	—	5.5	V	
D133	T_{PEW}	Erase/Write cycle time	—	4	8	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may choose the better of the two specs.

9.3 AC (Timing) Characteristics

9.3.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	os, osc	OSC1
ck	CLKOUT	ost	oscillator start-up timer
cy	cycle time	pwrt	power-up timer
io	I/O port	rbt	RBx pins
inp	INT pin	t0	T0CKI
mp	$\overline{\text{MCLR}}$	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (high impedance)	V	Valid
L	Low	Z	High Impedance

9.3.2 TIMING CONDITIONS

The temperature and voltages specified in Table 9-1 apply to all timing specifications unless otherwise noted. All timings are measured between high and low measurement points as indicated in Figure 9-4. Figure 9-5 specifies the load conditions for the timing specifications.

TABLE 9-1: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

AC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ T_A ≤ +70°C for commercial -40°C ≤ T_A ≤ +85°C for industrial Operating voltage V_{DD} range as described in DC specifications (Section 9.1)

FIGURE 9-4: PARAMETER MEASUREMENT INFORMATION

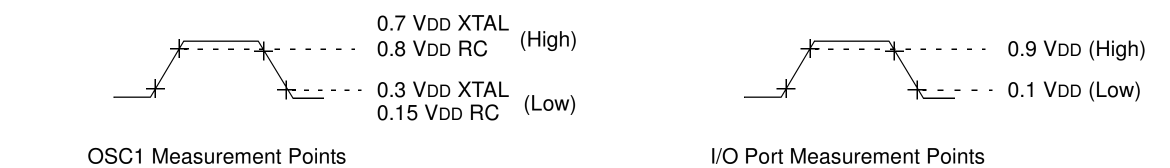


FIGURE 9-5: LOAD CONDITIONS

R_L =	464Ω	
C_L =	50 pF	for all pins except OSC2
	15 pF	for OSC2 output

9.3.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 9-6: EXTERNAL CLOCK TIMING

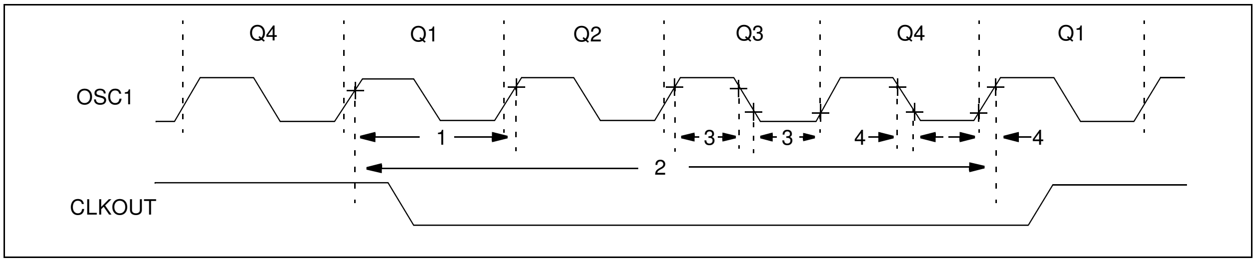


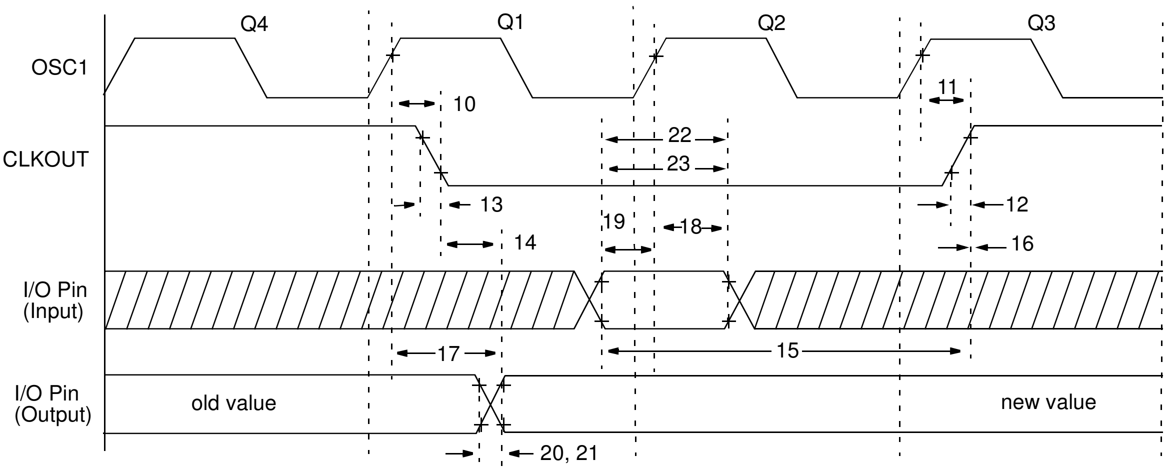
TABLE 9-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
	FOSC	**External CLKIN Frequency(1)**	DC	—	2	MHz	XT, RC osc	(-04, LF)
			DC	—	4	MHz	XT, RC osc	(-04)
			DC	—	20	MHz	HS osc	(-20)
			DC	—	200	kHz	LP osc	(-04, LF)
		Oscillator Frequency(1)	DC	—	2	MHz	RC osc	(-04, LF)
			DC	—	4	MHz	RC osc	(-04)
			0.1	—	2	MHz	XT osc	(-04, LF)
			0.1	—	4	MHz	XT osc	(-04)
			1.0	—	20	MHz	HS osc	(-20)
			DC	—	200	kHz	LP osc	(-04, LF)
1	TOSC	**External CLKIN Period(1)**	500	—	—	ns	XT, RC osc	(-04, LF)
			250	—	—	ns	XT, RC osc	(-04)
			50	—	—	ns	HS osc	(-20)
			5.0	—	—	μs	LP osc	(-04, LF)
		Oscillator Period(1)	500	—	—	ns	RC osc	(-04, LF)
			250	—	—	ns	RC osc	(-04)
			500	—	10,000	ns	XT osc	(-04, LF)
			250	—	10,000	ns	XT osc	(-04)
			50	—	1,000	ns	HS osc	(-20)
			5.0	—	—	μs	LP osc	(-04, LF)
2	TCY	**Instruction Cycle Time(1)**	0.2	4/FOSC	DC	μs		
3	TosL, TosH	**Clock in (OSC1) High or Low Time**	60	—	—	ns	XT osc	(-04, LF)
			50	—	—	ns	XT osc	(-04)
			2.0	—	—	μs	LP osc	(-04, LF)
			17.5	—	—	ns	HS osc	(-20)
4	TosR, TosF	**Clock in (OSC1) Rise or Fall Time**	25	—	—	ns	XT osc	(-04)
			50	—	—	ns	LP osc	(-04, LF)
			7.5	—	—	ns	HS osc	(-20)

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 9-7: CLKOUT AND I/O TIMING



Note: All tests must be done with specified capacitive loads (Figure 9-5) 50 pF on I/O pins and CLKOUT.

TABLE 9-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	Standard	—	15	30	ns	**(Note 1)**
10A			Extended (LF)	—	15	120	ns	**(Note 1)**
11	TosH2ckH	OSC1↑ to CLKOUT↑	Standard	—	15	30	ns	**(Note 1)**
11A			Extended (LF)	—	15	120	ns	**(Note 1)**
12	TckR	CLKOUT rise time	Standard	—	15	30	ns	**(Note 1)**
12A			Extended (LF)	—	15	100	ns	**(Note 1)**
13	TckF	CLKOUT fall time	Standard	—	15	30	ns	**(Note 1)**
13A			Extended (LF)	—	15	100	ns	**(Note 1)**
14	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY +20	ns	**(Note 1)**
15	TioV2ckH	Port in valid before CLKOUT ↑	Standard	0.30TCY + 30	—	—	ns	**(Note 1)**
			Extended (LF)	0.30TCY + 80	—	—	ns	**(Note 1)**
16	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	**(Note 1)**
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	Standard	—	—	125	ns	
			Extended (LF)	—	—	250	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	Standard	10	—	—	ns	
			Extended (LF)	10	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	Standard	-75	—	—	ns	
			Extended (LF)	-175	—	—	ns	
20	TioR	Port output rise time	Standard	—	10	35	ns	
20A			Extended (LF)	—	10	70	ns	
21	TioF	Port output fall time	Standard	—	10	35	ns	
21A			Extended (LF)	—	10	70	ns	
22	TINP	INT pin high or low time	Standard	20	—	—	ns	
22A			Extended (LF)	55	—	—	ns	
23	TRBP	RB7:RB4 change INT high or low time	Standard	TOSC§	—	—	ns	
23A			Extended (LF)	TOSC§	—	—	ns	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
§ By design.
Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 9-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

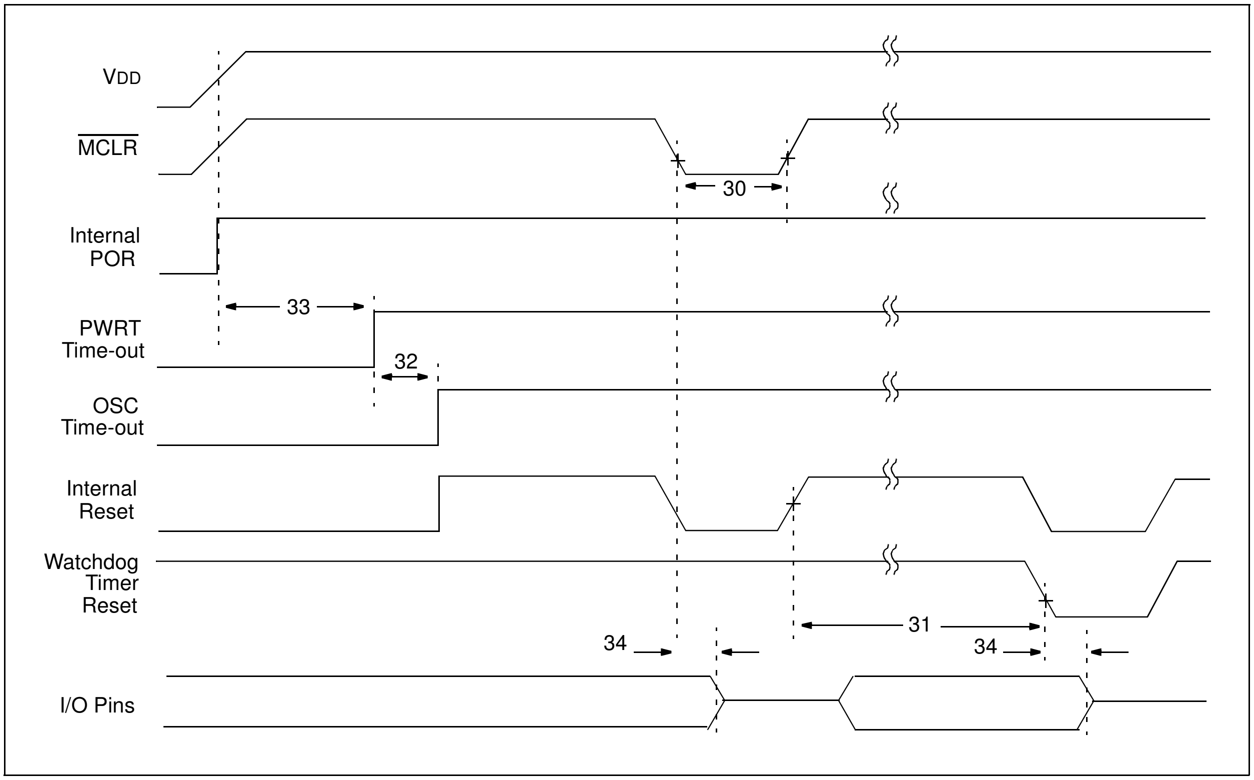


TABLE 9-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	VDD = 5.0V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5.0V
32	TOST	Oscillation Start-up Timer Period		1024TOSC		ms	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	28	72	132	ms	VDD = 5.0V
34	TIOZ	I/O hi-impedance from $\overline{\text{MCLR}}$ Low or RESET	—	—	100	ns	

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 9-9: TIMER0 CLOCK TIMINGS

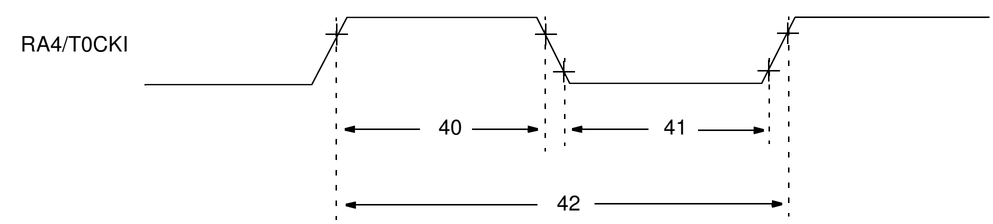


TABLE 9-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	50 30	— —	— —	ns ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	50 20	— —	— —	ns ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
42	Tt0P	T0CKI Period		$\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

10.0 DC/AC CHARACTERISTIC GRAPHS

The graphs provided in this section are for **design guidance** and are **not tested**.

In some graphs, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C. 'Max' or 'Min' represents (mean + 3σ) or (mean - 3σ), respectively, where σ is a standard deviation over the whole temperature range.

FIGURE 10-1: TYPICAL IDD vs. FOSC OVER VDD (HS MODE, 25°C)

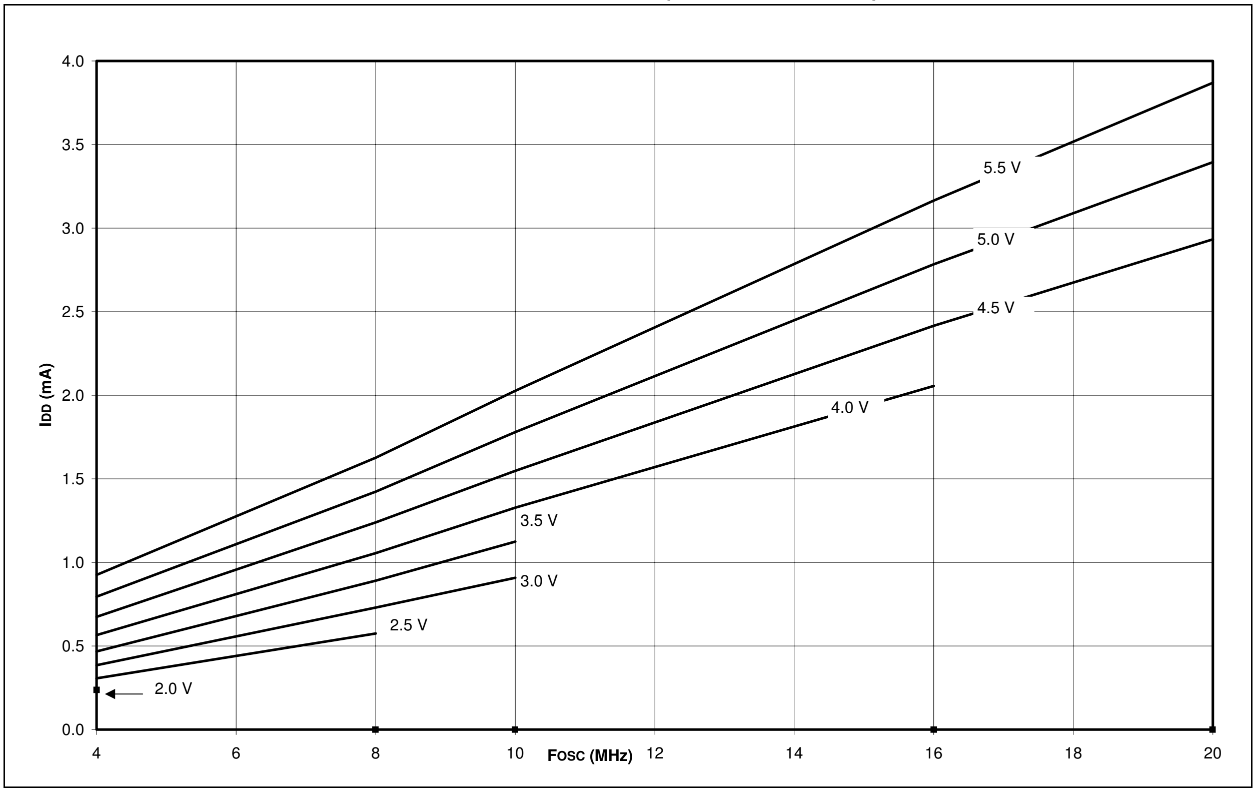


FIGURE 10-2: MAXIMUM IDD vs. FOSC OVER VDD (HS MODE, -40° TO +125°C)

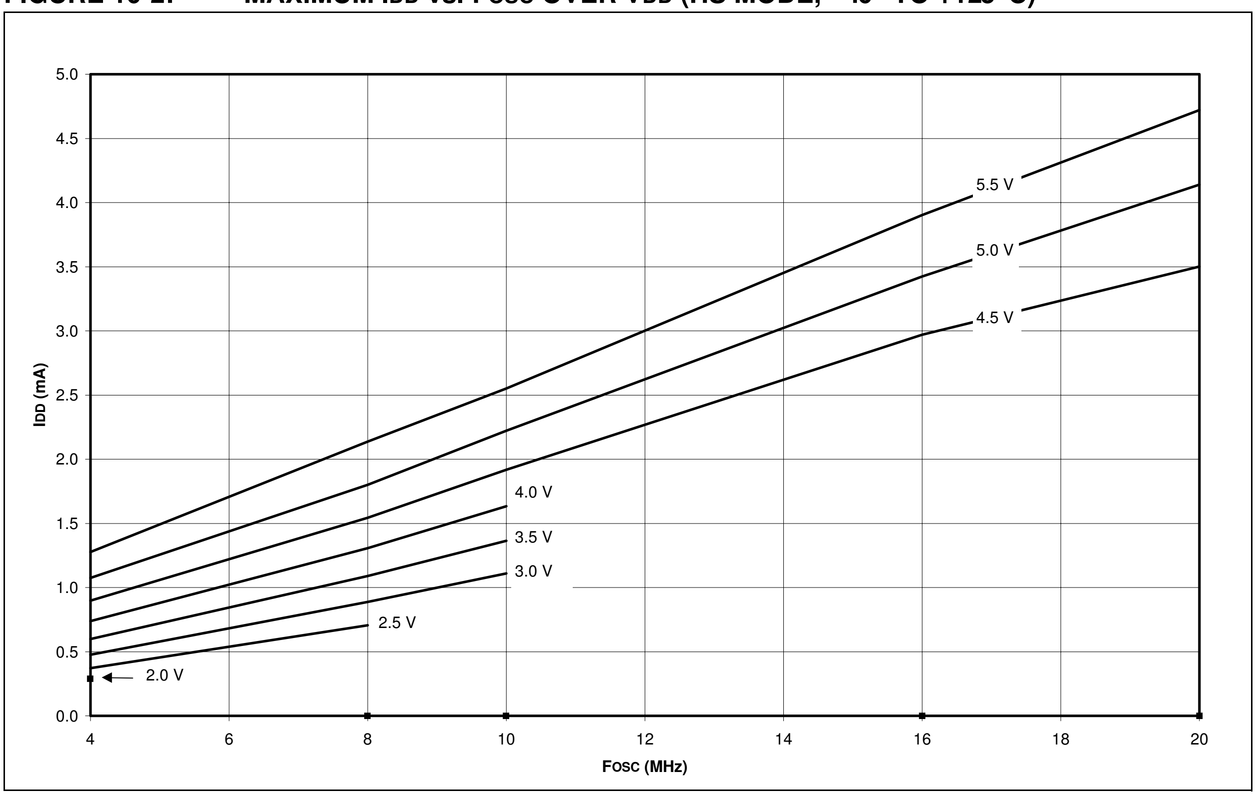


FIGURE 10-3: TYPICAL IDD vs. FOSC OVER VDD (XT MODE, 25°C)

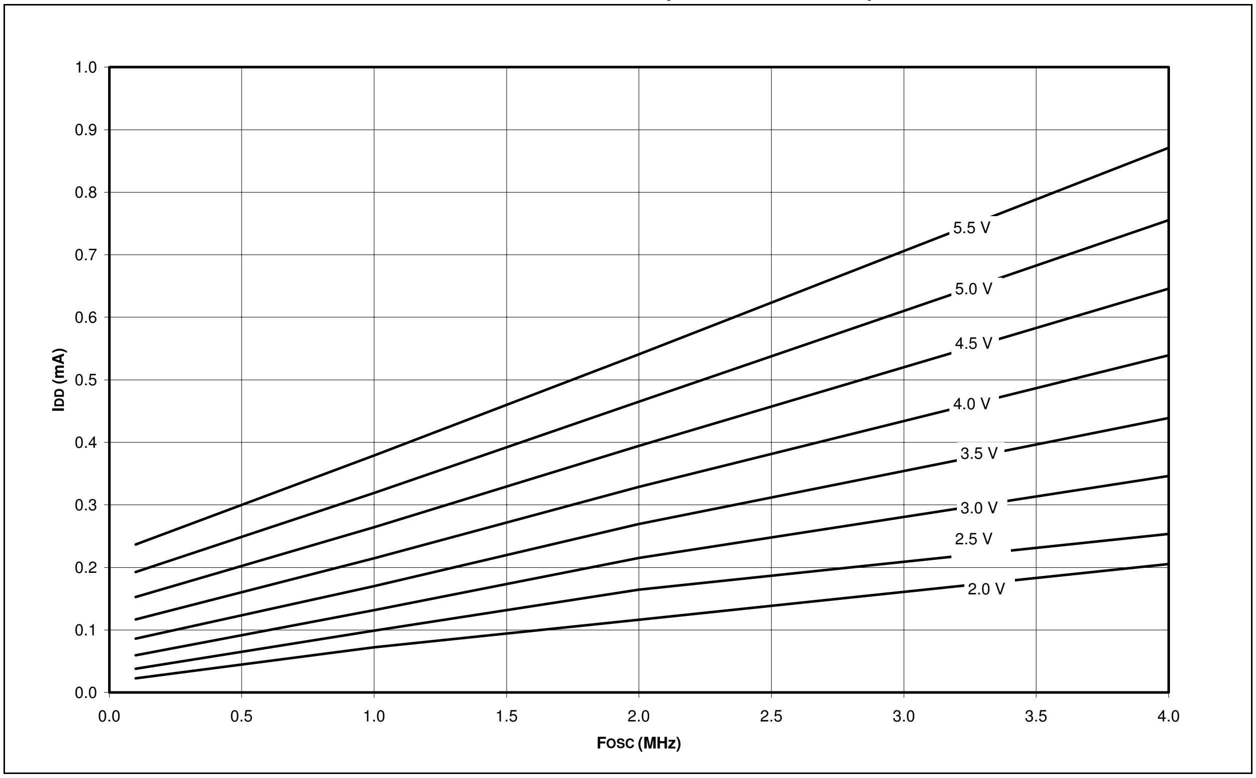


FIGURE 10-4: MAXIMUM IDD vs. FOSC OVER VDD (XT MODE, -40° TO +125°C)

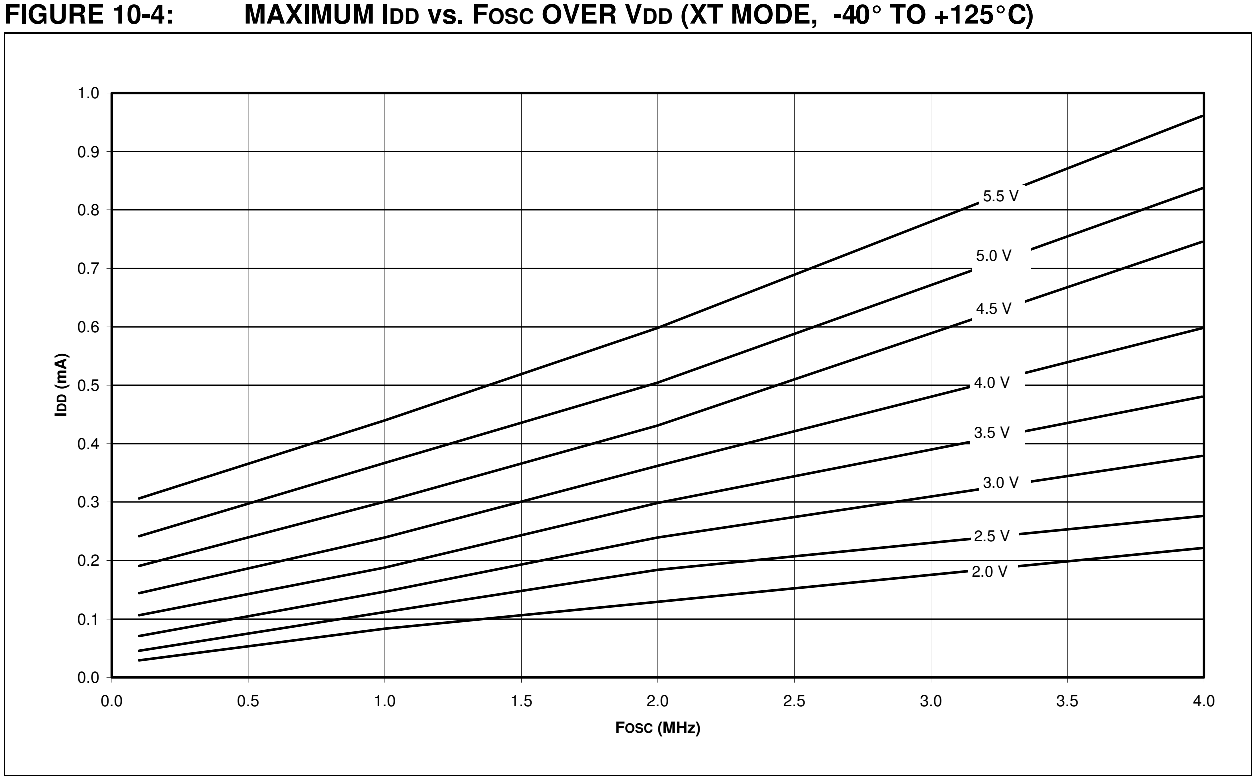


FIGURE 10-5: TYPICAL IDD vs. FOSC OVER VDD (LP MODE, 25°C)

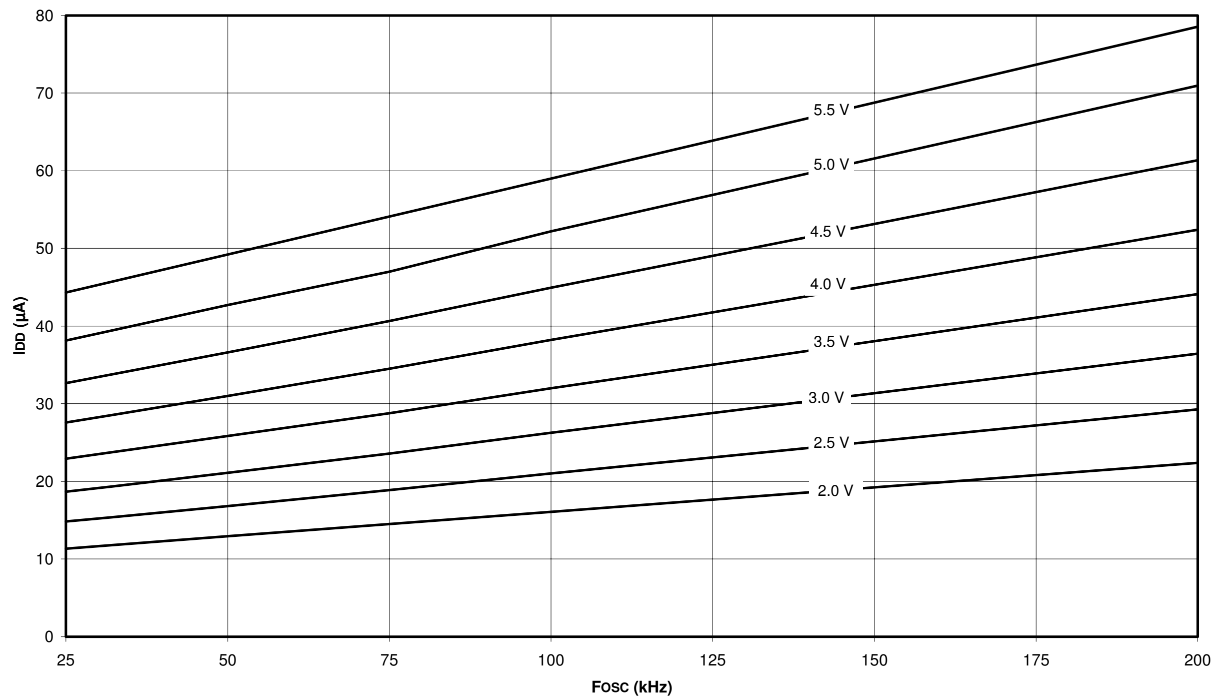


FIGURE 10-6: MAXIMUM IDD vs. FOSC OVER VDD (LP MODE, -40° TO +125°C)

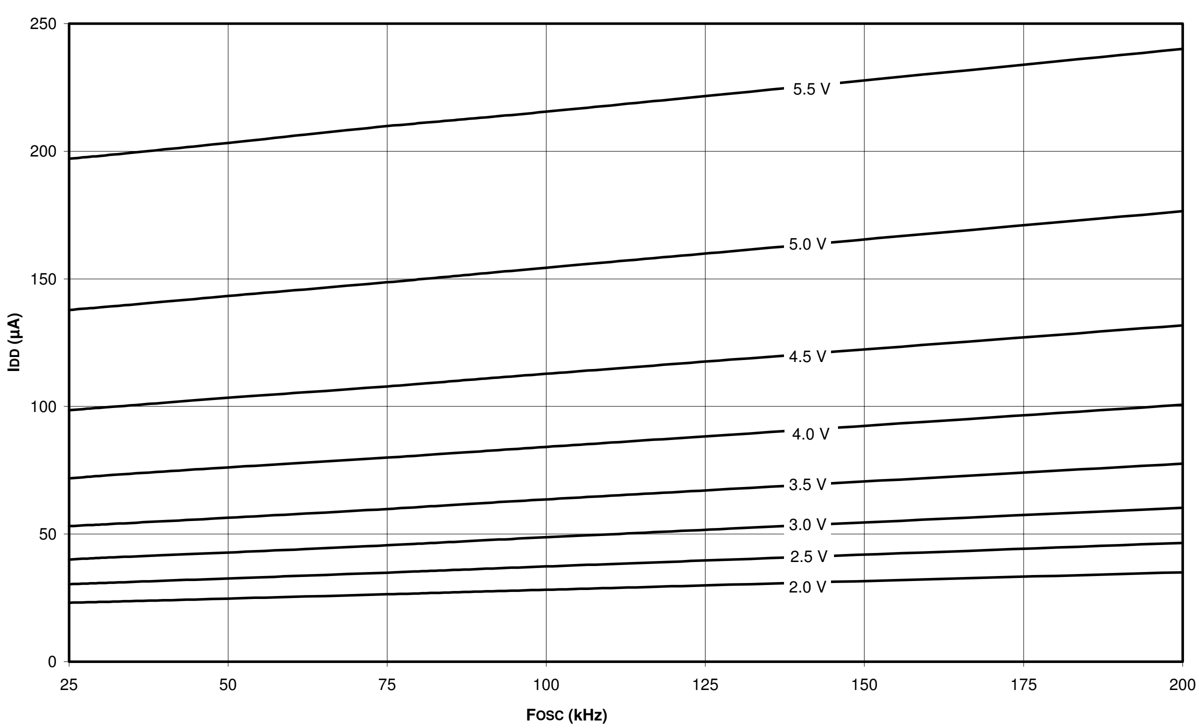


FIGURE 10-7: AVERAGE F_{OSC} vs. V_{DD} FOR R (RC MODE, C = 22 pF, 25°C)

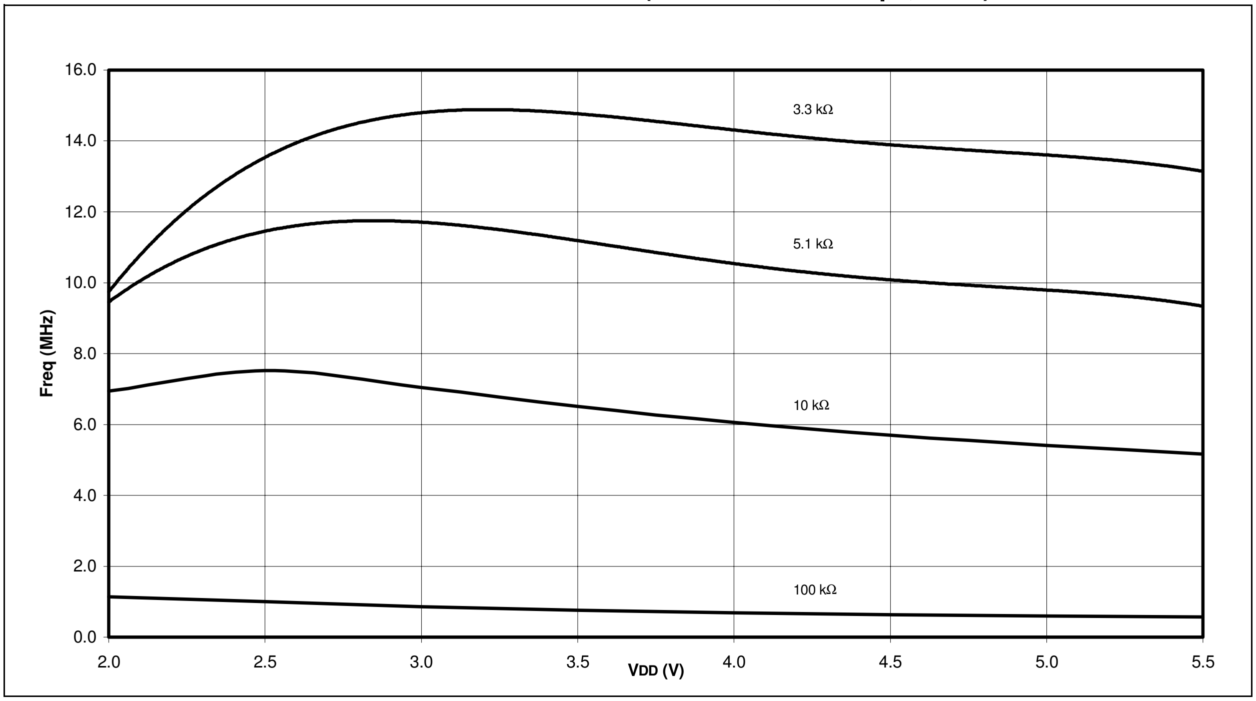


FIGURE 10-8: AVERAGE F_{OSC} vs. V_{DD} FOR R (RC MODE, C = 100 pF, 25°C)

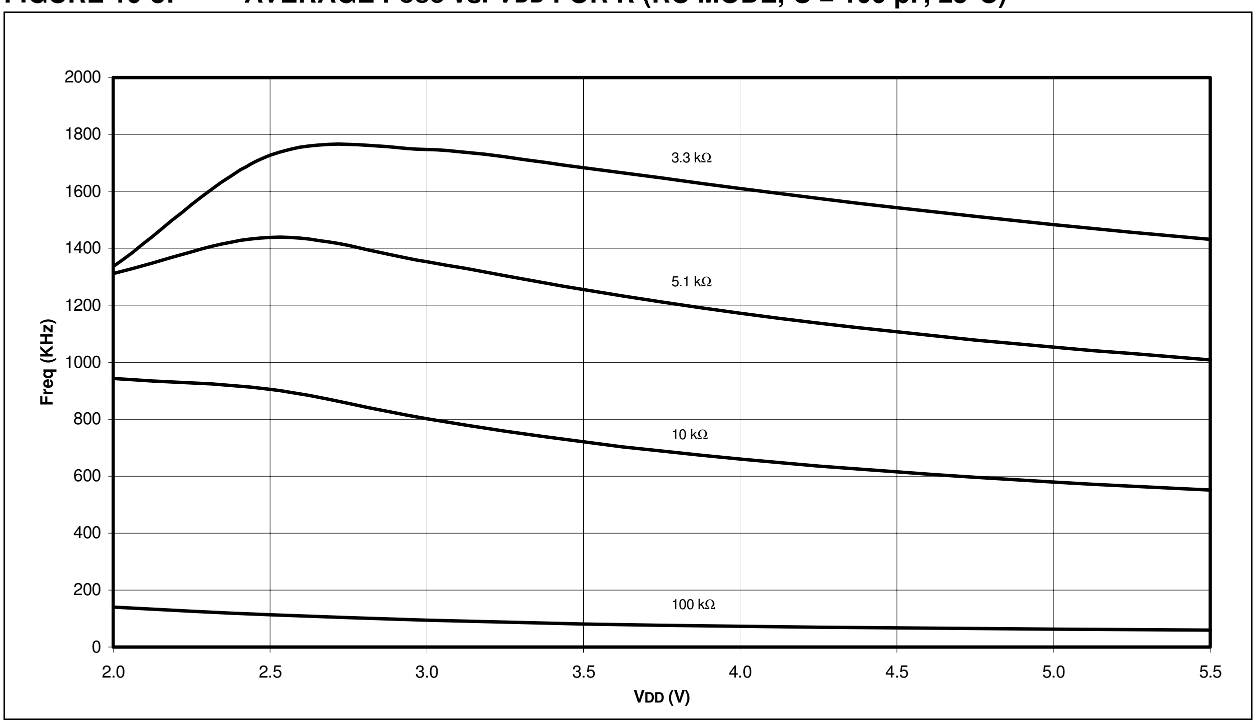


FIGURE 10-9: AVERAGE FOSC vs. VDD FOR R (RC MODE, C = 300 pF, 25°C)

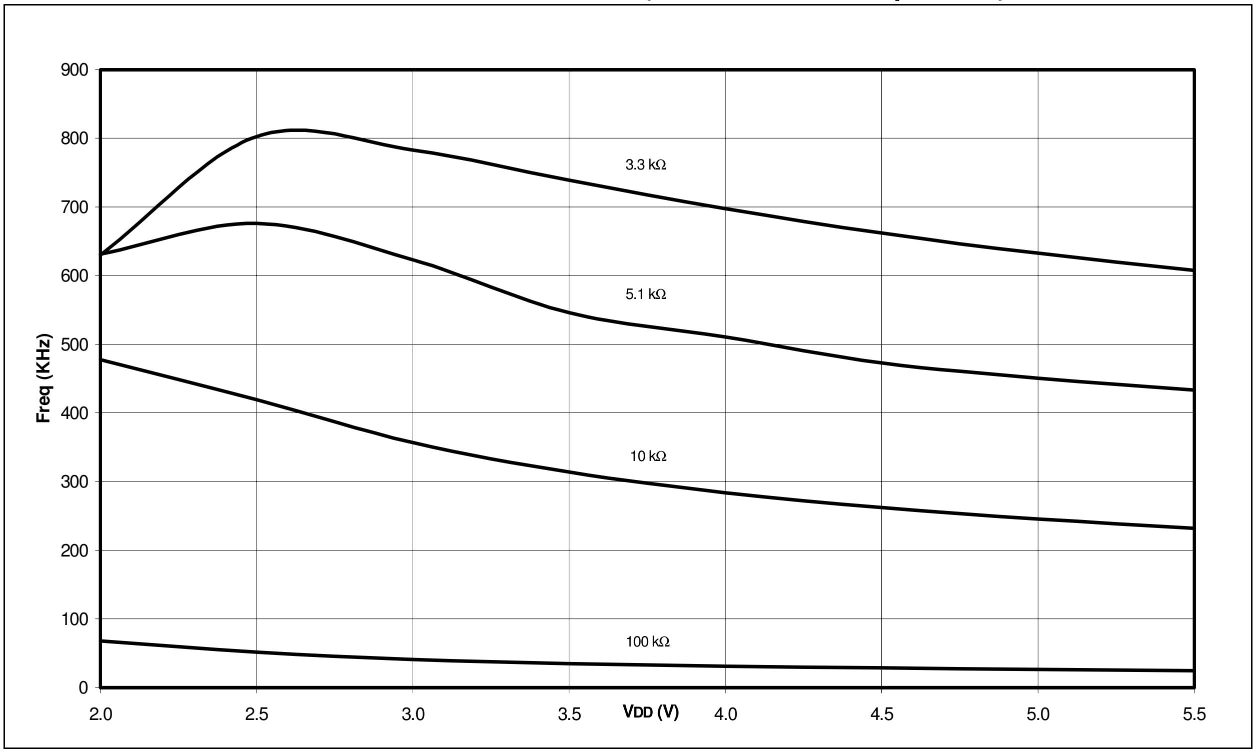


FIGURE 10-10: IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

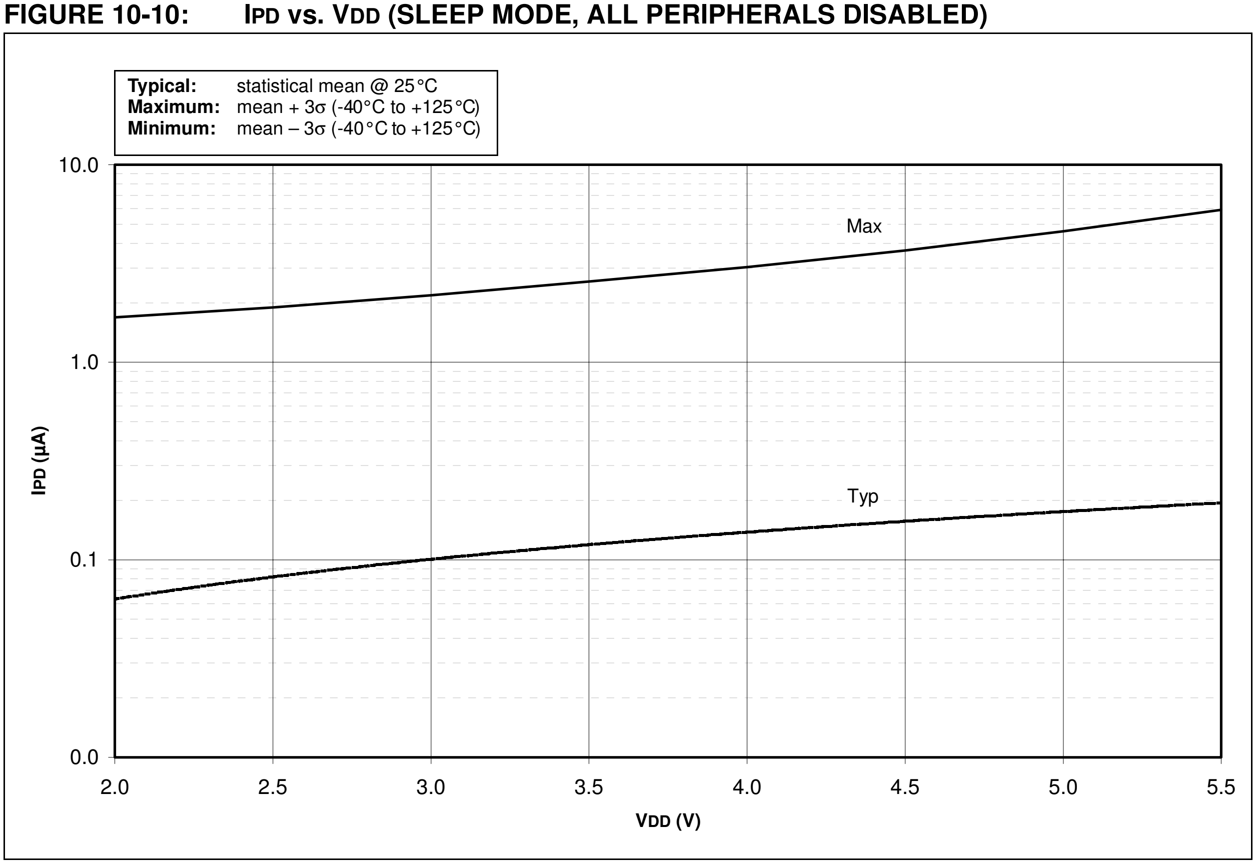


FIGURE 10-11: IPD vs. VDD (WDT MODE)

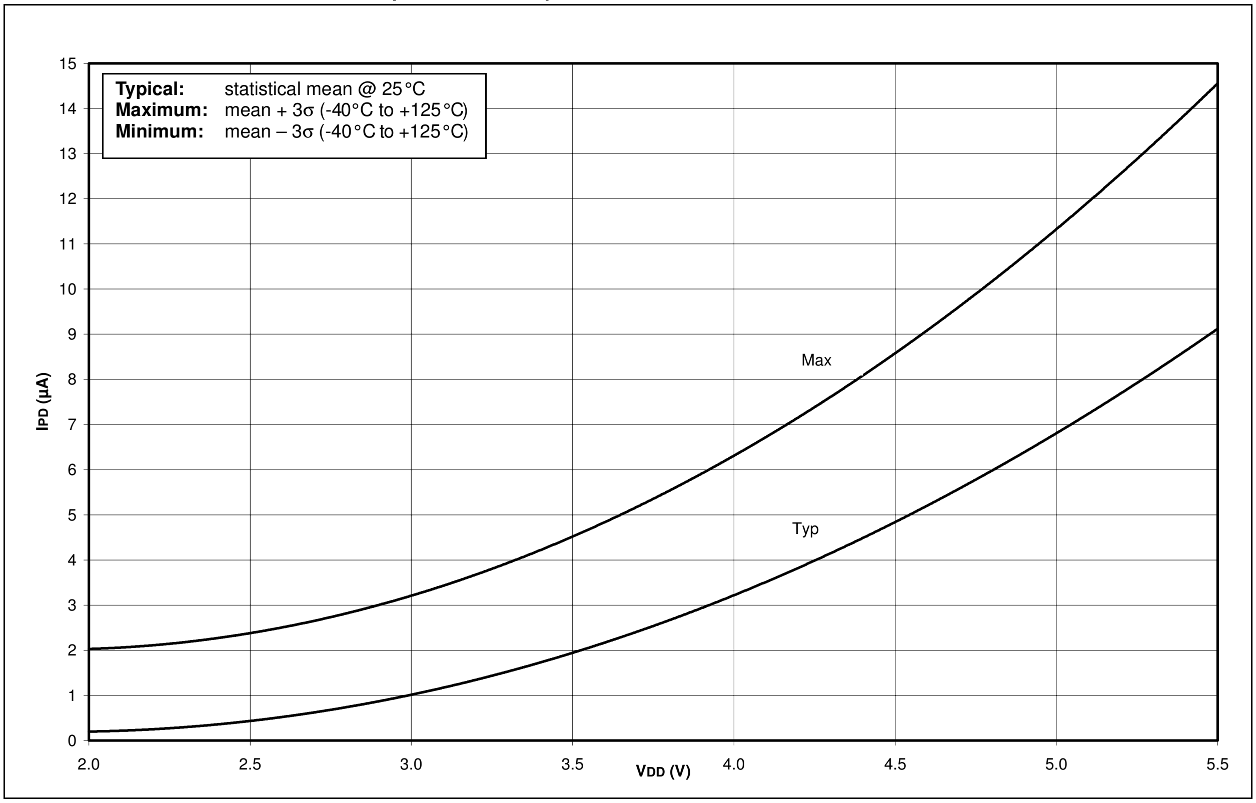


FIGURE 10-12: TYPICAL, MINIMUM, AND MAXIMUM WDT PERIOD vs. VDD OVER TEMP

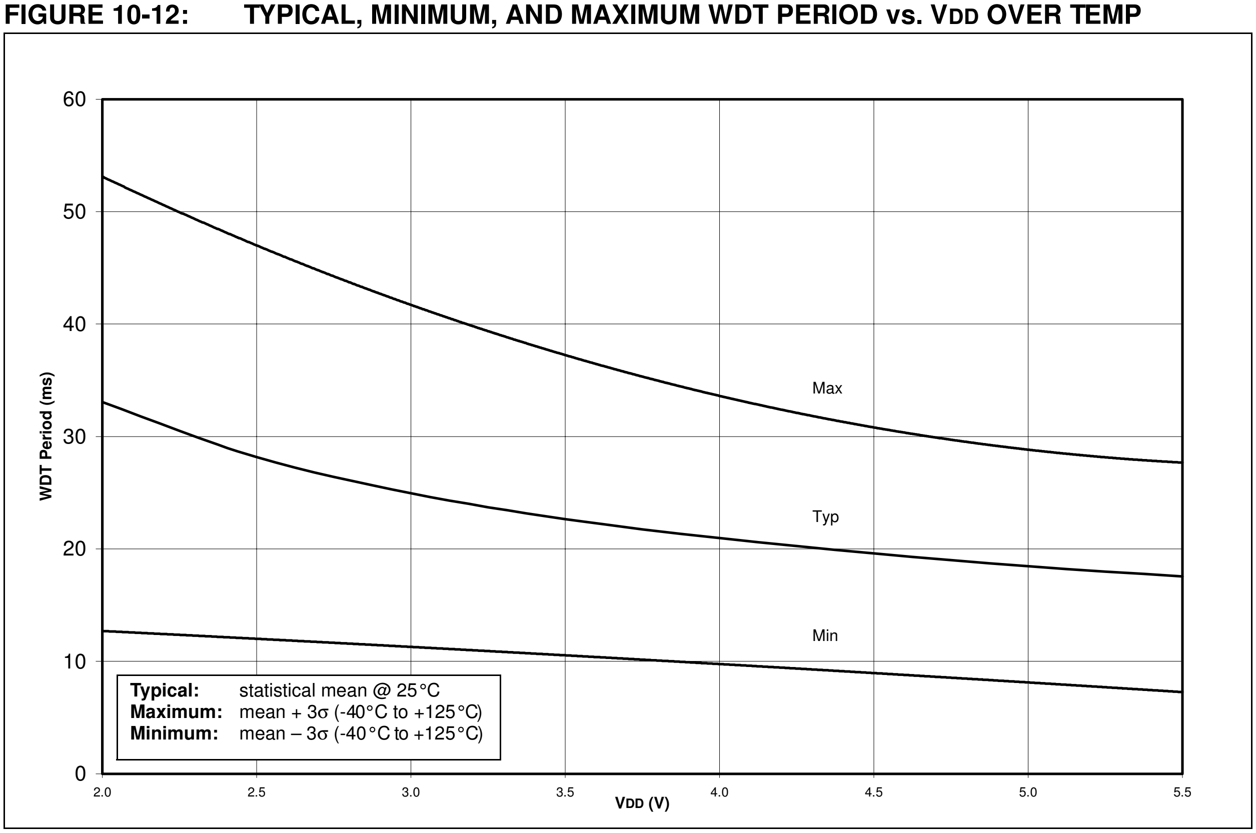


FIGURE 10-13: TYPICAL, MINIMUM AND MAXIMUM V_{OH} vs. I_{OH} (V_{DD} = 5V, -40°C TO +125°C)

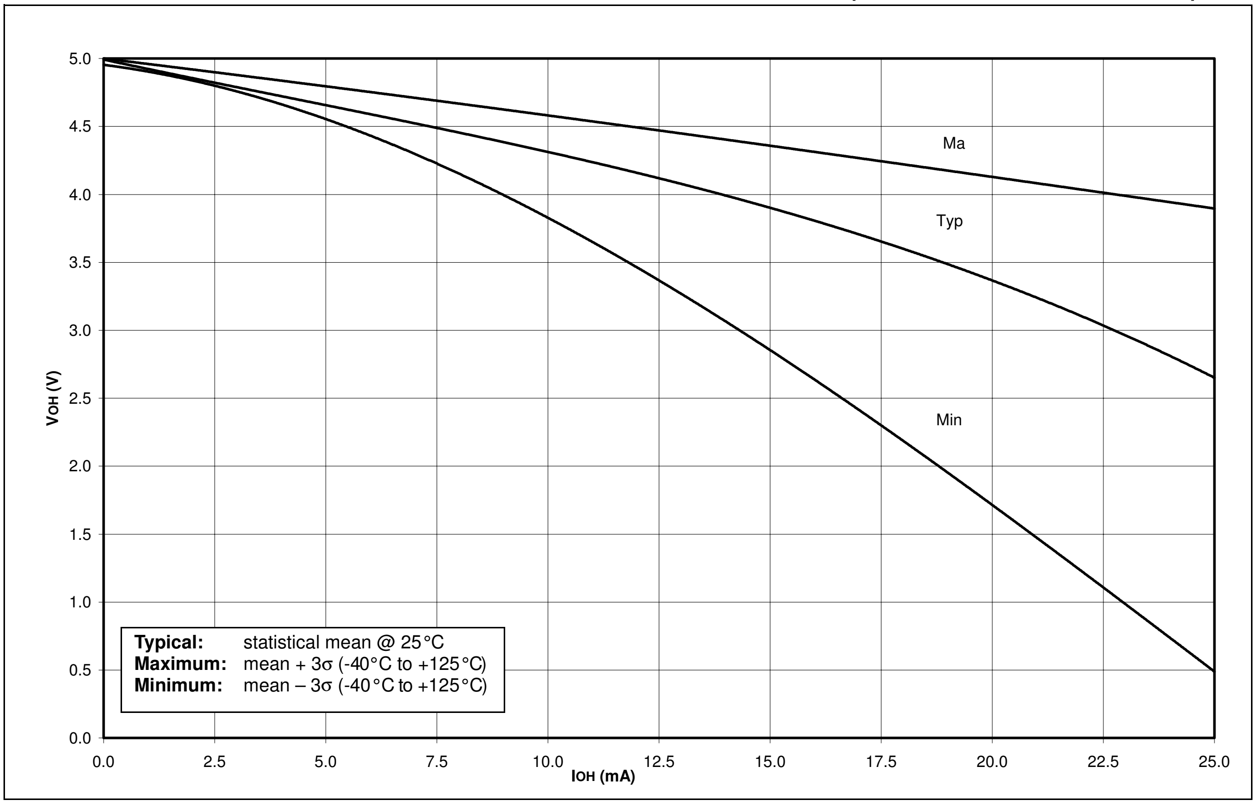


FIGURE 10-14: TYPICAL, MINIMUM AND MAXIMUM V_{OH} vs. I_{OH} (V_{DD} = 3V, -40°C TO +125°C)

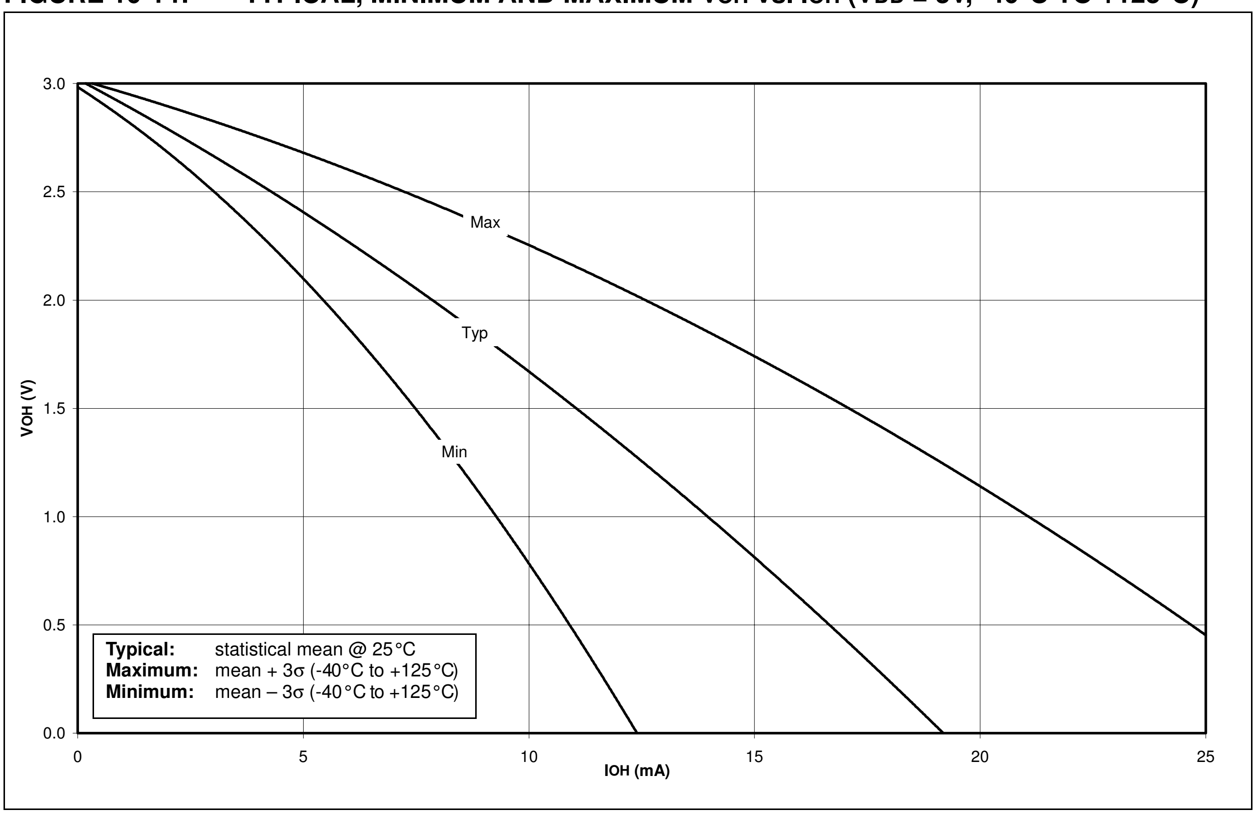


FIGURE 10-15: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 5V, -40°C TO +125°C)

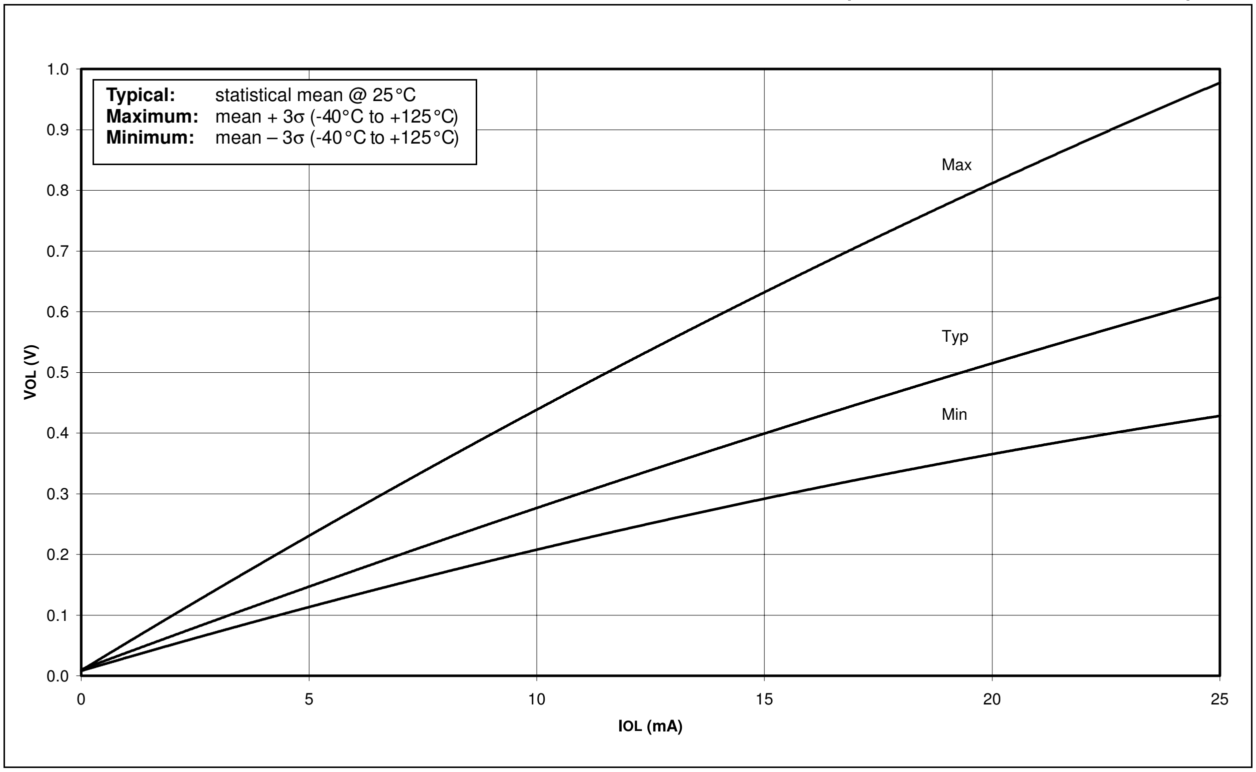


FIGURE 10-16: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 3V, -40°C TO +125°C)

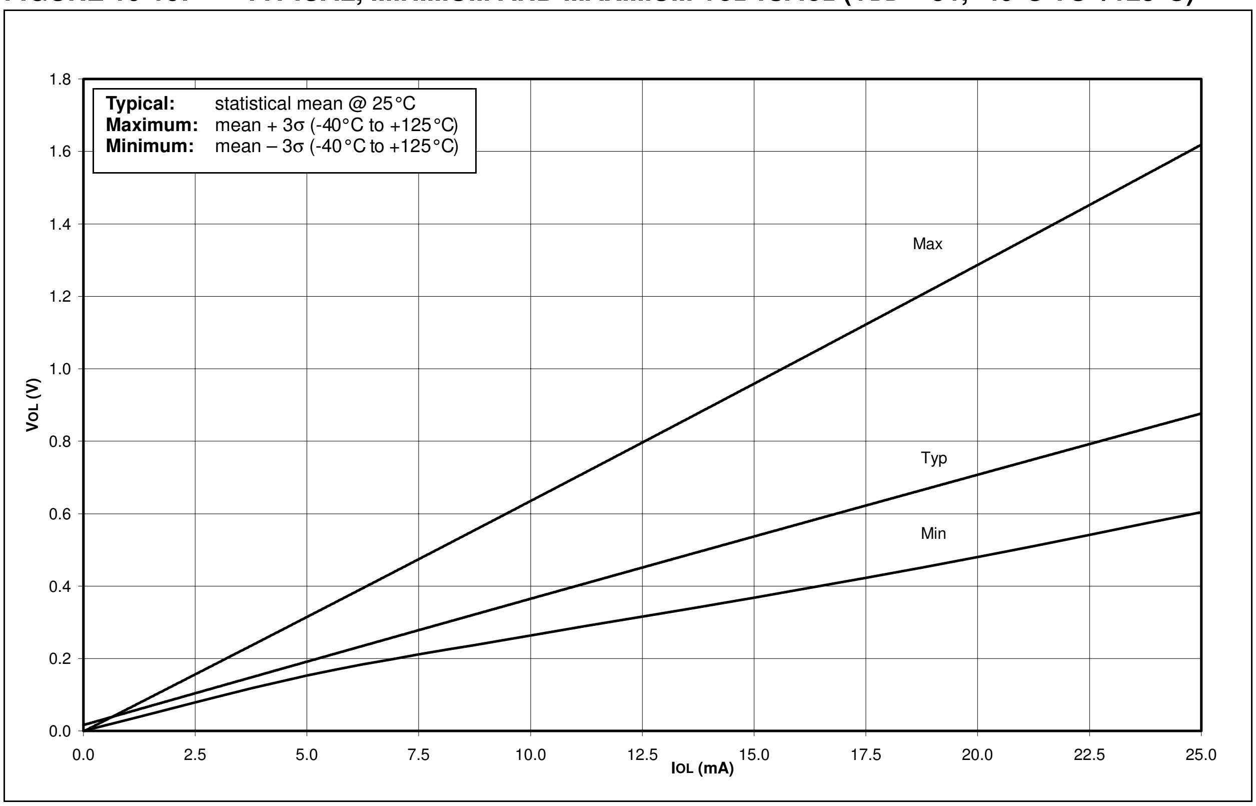


FIGURE 10-17: MINIMUM AND MAXIMUM VIN vs. VDD, (TTL INPUT, -40°C TO +125°C)

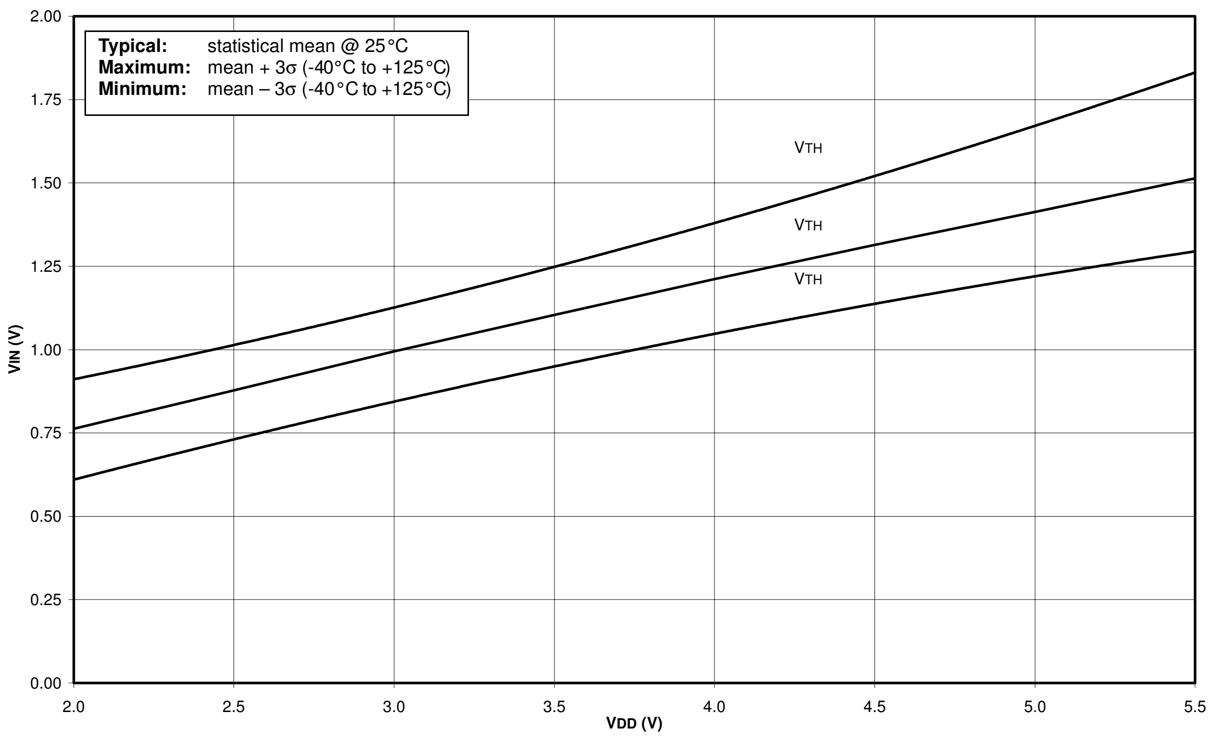
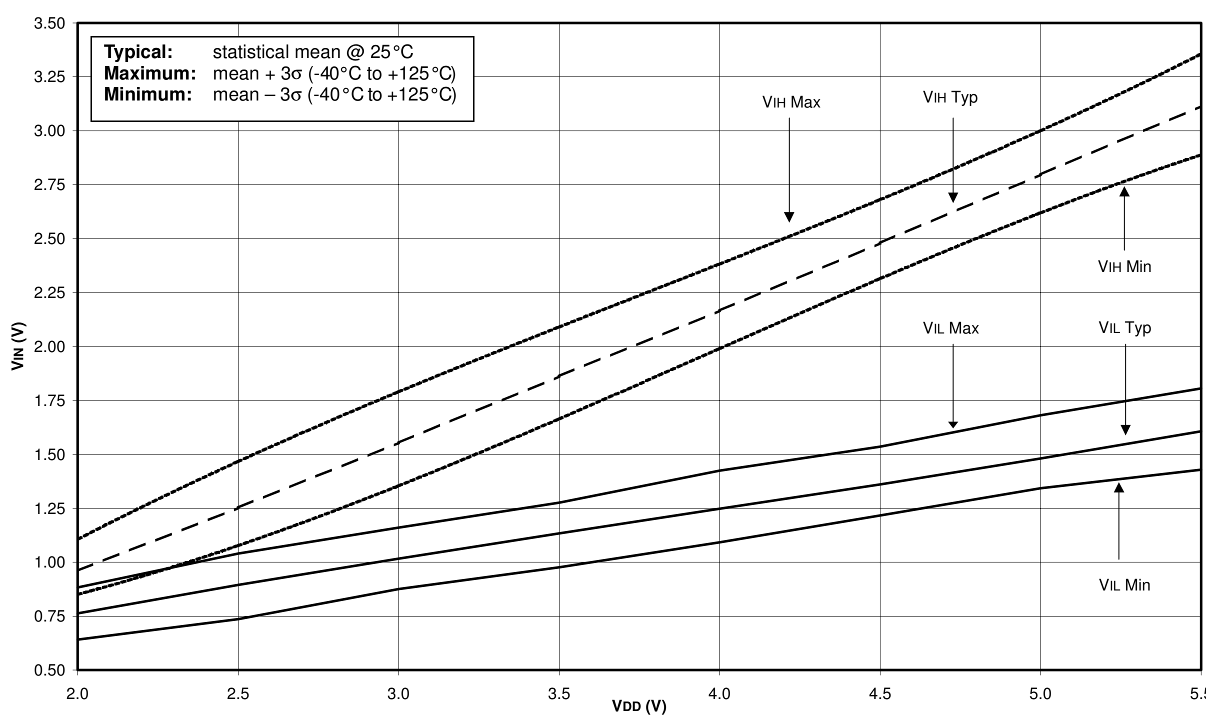


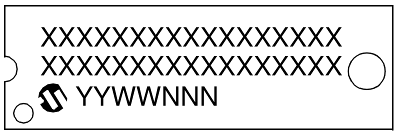
FIGURE 10-18: MINIMUM AND MAXIMUM VIN vs. VDD (ST INPUT, -40°C TO +125°C)



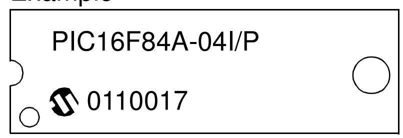
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

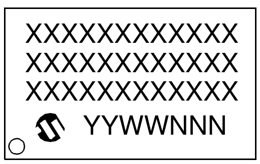
18-Lead PDIP



Example

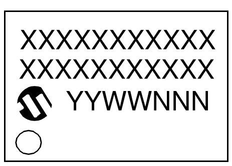


18-Lead SOIC

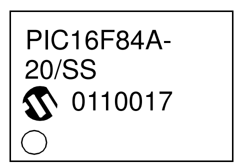


Example

20-Lead SSOP



Example

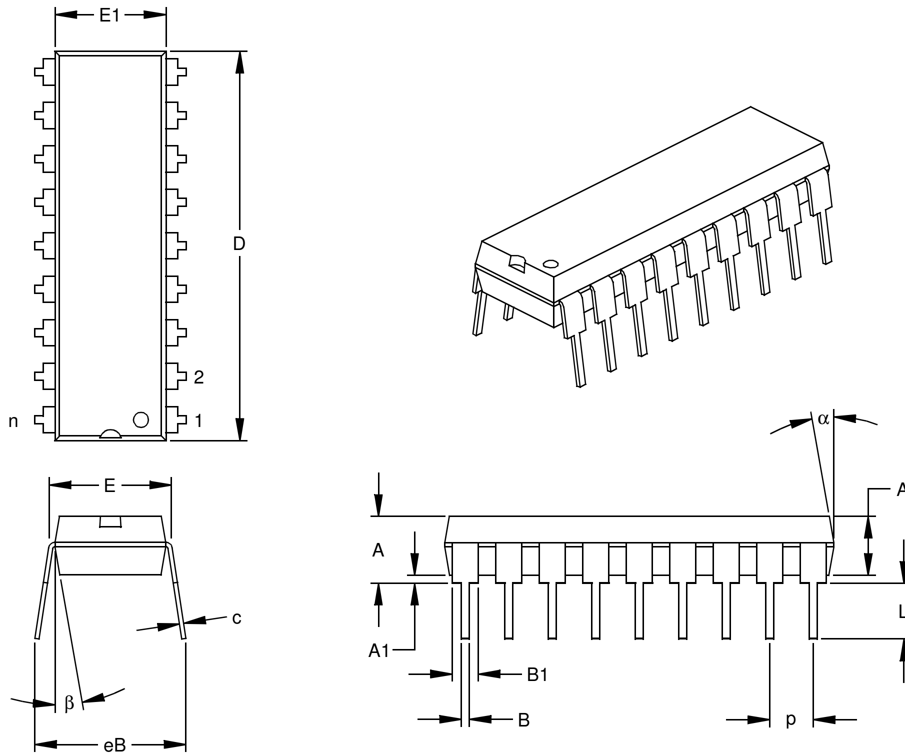


Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip sales office. For QTP devices, any special marking adders are included in QTP price.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

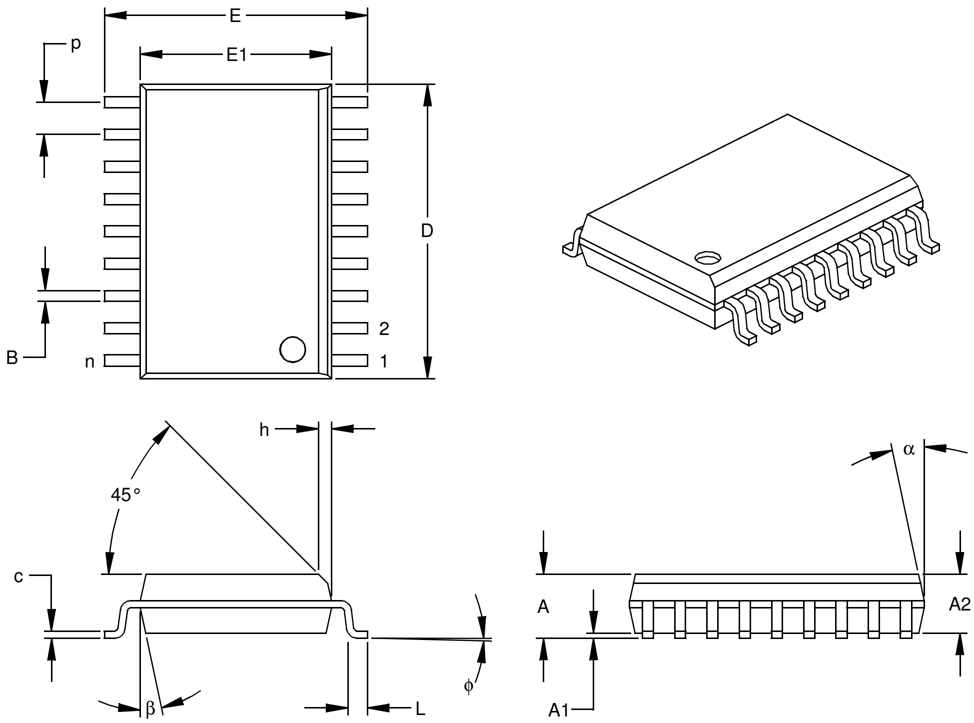


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

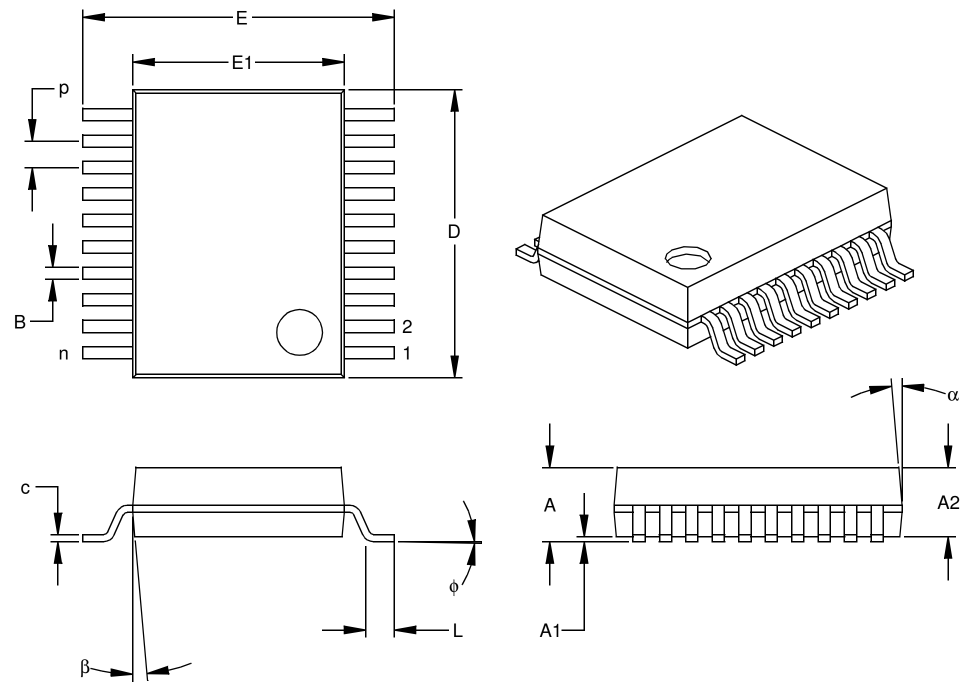


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	9/98	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the *PIC16F8X Data Sheet*, DS30430.
B	8/01	Added DC and AC Characteristics Graphs and Tables to Section 10.

APPENDIX B: CONVERSION CONSIDERATIONS

Considerations for converting from one PIC16X8X device to another are listed in Table 1.

TABLE 1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/ CR84	PIC16F84A
Program Memory Size	1K x 14	512 x 14 / 1K x 14	512 x 14 / 1K x 14	1K x 14
Data Memory Size	36 x 8	36 x 8 / 68 x 8	36 x 8 / 68 x 8	68 x 8
Voltage Range	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 5.5V (-40°C to +125°C)
Maximum Operating Frequency	10 MHz	10 MHz	10 MHz	20 MHz
Supply Current (I_{DD}). See parameter # D014 in the electrical specs for more detail.	I_{DD} (typ) = 60 μA I_{DD} (max) = 400 μA (LP osc, F_{OSC} = 32 kHz, V_{DD} = 2.0V, WDT disabled)	I_{DD} (typ) = 15 μA I_{DD} (max) = 45 μA (LP osc, F_{OSC} = 32 kHz, V_{DD} = 2.0V, WDT disabled)	I_{DD} (typ) = 15 μA I_{DD} (max) = 45 μA (LP osc, F_{OSC} = 32 kHz, V_{DD} = 2.0V, WDT disabled)	I_{DD} (typ) = 15 μA I_{DD} (max) = 45 μA (LP osc, F_{OSC} = 32 kHz, V_{DD} = 2.0V, WDT disabled)
Power-down Current (I_{PD}). See parameters # D020, D021, and D021A in the electrical specs for more detail.	I_{PD} (typ) = 26 μA I_{PD} (max) = 100 μA (V_{DD} = 2.0V, WDT disabled, industrial)	I_{PD} (typ) = 0.4 μA I_{PD} (max) = 9 μA (V_{DD} = 2.0V, WDT disabled, industrial)	I_{PD} (typ) = 0.4 μA I_{PD} (max) = 6 μA (V_{DD} = 2.0V, WDT disabled, industrial)	I_{PD} (typ) = 0.4 μA I_{PD} (max) = 1 μA (V_{DD} = 2.0V, WDT disabled, industrial)
Input Low Voltage (V_{IL}). See parameters # D032 and D034 in the electrical specs for more detail.	V_{IL} (max) = 0.2V_{DD} (OSC1, RC mode)	V_{IL} (max) = 0.1V_{DD} (OSC1, RC mode)	V_{IL} (max) = 0.1V_{DD} (OSC1, RC mode)	V_{IL} (max) = 0.1V_{DD} (OSC1, RC mode)
Input High Voltage (V_{IH}). See parameter # D040 in the electrical specs for more detail.	V_{IH} (min) = 0.36V_{DD} (I/O Ports with TTL, 4.5V ≤ V_{DD} ≤ 5.5V)	V_{IH} (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ V_{DD} ≤ 5.5V)	V_{IH} (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ V_{DD} ≤ 5.5V)	V_{IH} (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ V_{DD} ≤ 5.5V)
Data EEPROM Memory Erase/Write cycle time (T_{DEW}). See parameter # D122 in the electrical specs for more detail.	T_{DEW} (typ) = 10 ms T_{DEW} (max) = 20 ms	T_{DEW} (typ) = 10 ms T_{DEW} (max) = 20 ms	T_{DEW} (typ) = 10 ms T_{DEW} (max) = 20 ms	T_{DEW} (typ) = 4 ms T_{DEW} (max) = 8 ms
Port Output Rise/Fall time (TioR, TioF). See parameters #20, 20A, 21, and 21A in the electrical specs for more detail.	TioR, TioF (max) = 25 ns (C84) TioR, TioF (max) = 60 ns (LC84)	TioR, TioF (max) = 35 ns (C84) TioR, TioF (max) = 70 ns (LC84)	TioR, TioF (max) = 35 ns (C84) TioR, TioF (max) = 70 ns (LC84)	TioR, TioF (max) = 35 ns (C84) TioR, TioF (max) = 70 ns (LC84)
$\overline{\text{MCLR}}$ on-chip filter. See parameter #30 in the electrical specs for more detail.	No	Yes	Yes	Yes
PORTA and crystal oscillator values less than 500 kHz	For crystal oscillator configurations operating below 500 kHz, the device may generate a spurious internal Q-clock when PORTA<0> switches state.	N/A	N/A	N/A
RB0/INT pin	TTL	TTL/ST* (*Schmitt Trigger)	TTL/ST* (*Schmitt Trigger)	TTL/ST* (*Schmitt Trigger)

TABLE 1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A (CONTINUED)

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/ CR84	PIC16F84A
EEADR<7:6> and I_{DD}	It is recommended that the EEADR<7:6> bits be cleared. When either of these bits is set, the maximum I_{DD} for the device is higher than when both are cleared.	N/A	N/A	N/A
The polarity of the $\overline{\text{PWRTE}}$ bit	PWRTE	$\overline{\text{PWRTE}}$	$\overline{\text{PWRTE}}$	$\overline{\text{PWRTE}}$
Recommended value of R_{EXT} for RC oscillator circuits	R_{EXT} = 3kΩ - 100kΩ	R_{EXT} = 5kΩ - 100kΩ	R_{EXT} = 5kΩ - 100kΩ	R_{EXT} = 3kΩ - 100kΩ
GIE bit unintentional enable	If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction).	N/A	N/A	N/A
Packages	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC, SSOP
Open Drain High Voltage (V_{OD})	14V	12V	12V	8.5V

APPENDIX C: MIGRATION FROM BASELINE TO MID-RANGE DEVICES

This section discusses how to migrate from a baseline device (i.e., PIC16C5X) to a mid-range device (i.e., PIC16CXXX).

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes, both in program memory (2K now as opposed to 512K before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the STATUS register and placed in the OPTION register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: `RETURN`, `RETFIE`, `ADDLW`, and `SUBLW`. Two instructions, `TRIS` and `OPTION`, are being phased out, although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to eight-deep.
8. RESET vector is changed to 0000h.
9. RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt-on-change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: V_{DD}, V_{SS}, V_{PP}, RB6 (clock) and RB7 (data in/out).

To convert code written for PIC16C5X to PIC16F84A, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for `CALL`, `GOTO`.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to 0000h.

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NOTES:

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Device: PIC16F84A   Literature Number: DS35007B

Questions:

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____

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____

____

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PIC16F84A PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16F84A(1), PIC16F84AT(2) PIC16LF84A(1), PIC16LF84AT(2)
Frequency Range	04 = 4 MHz 20 = 20 MHz
Temperature Range	- = 0°C to +70°C I = -40°C to +85°C
Package	P = PDIP SO = SOIC (Gull Wing, 300 mil body) SS = SSOP
Pattern	QTP, SQTP, ROM Code (factory specified) or Special Requirements . Blank for OTP and Windowed devices.

Examples:

a) PIC16F84A -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.

b) PIC16LF84A - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended VDD limits.

c) PIC16F84A - 20I/P = Industrial temp., PDIP package, 20 MHz, normal VDD limits.

Note 1: F = Standard VDD range
LF = Extended VDD range
2: T = in tape and reel - SOIC and SSOP packages only.

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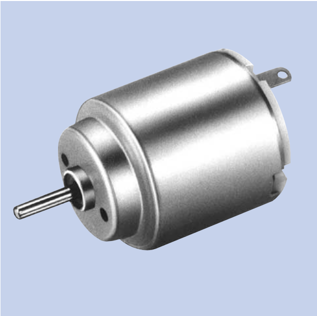
08/01/01

RE-140RA

MABUCHI MOTOR

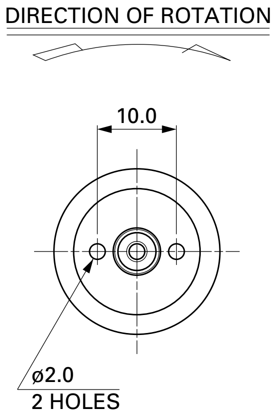
OUTPUT: APPROX 0.2W~3.0W *Metal-brush motors*

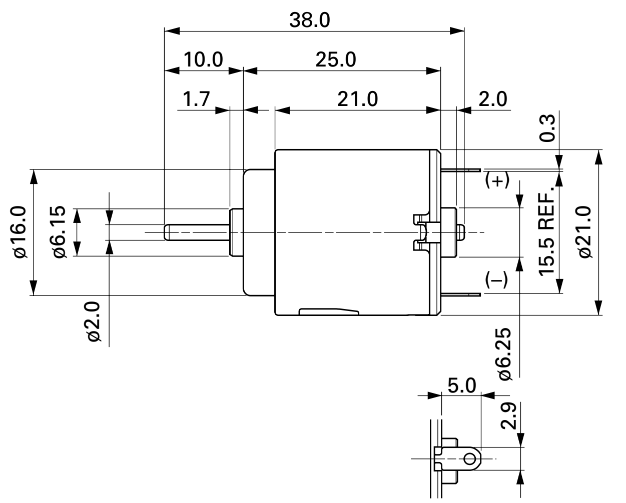
Typical Applications **Toys and Models :** Motorized Toy / Motorized Plastic Model

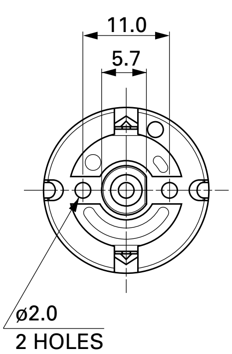


MODEL	VOLTAGE		NO LOAD		AT MAXIMUM EFFICIENCY					STALL		
	OPERATING RANGE	NOMINAL	SPEED	CURRENT	SPEED	CURRENT	TORQUE		OUTPUT	TORQUE		CURRENT
			r/min	A	r/min	A	mN·m	g·cm	W	mN·m	g·cm	A
RE-140RA-2270	1.5 ~ 3.0	1.5V CONSTANT	8100	0.21	6150	0.66	0.66	6.7	0.42	2.74	28	2.10
RE-140RA-18100	1.5 ~ 3.0	1.5V CONSTANT	5700	0.13	4230	0.37	0.48	4.9	0.21	1.86	19	1.07
RE-140RA-12240	3 ~ 6	3V CONSTANT	4800	0.050	3530	0.14	0.44	4.5	0.16	1.67	17	0.39

UNIT: MILLIMETERS

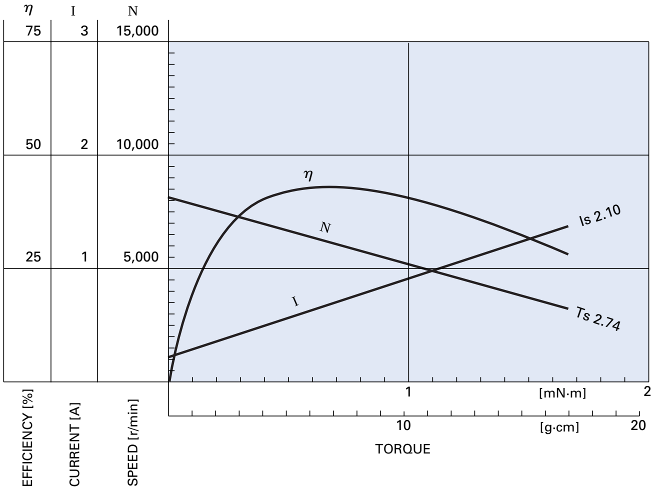




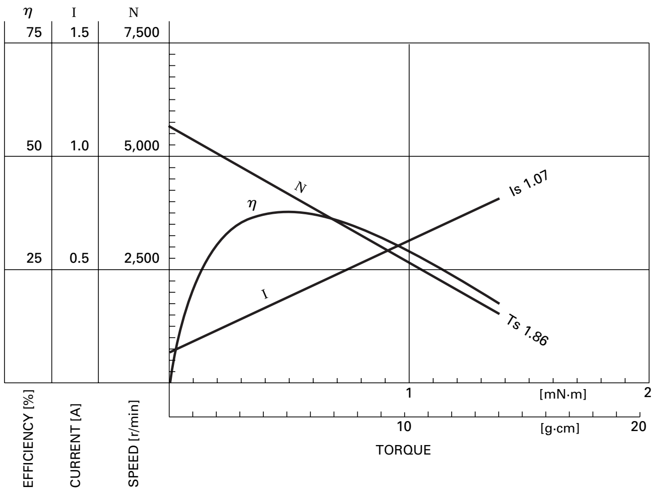


WEIGHT: 19g (APPROX)

RE-140RA-2270 1.5V

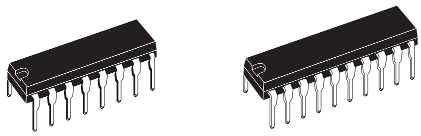


RE-140RA-18100 1.5V



PUSH-PULL FOUR CHANNEL DRIVERS

- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (non repetitive)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION



DIP16 **POWERDIP(16+2+2)**

ORDERING NUMBERS:

L293B **L293E**

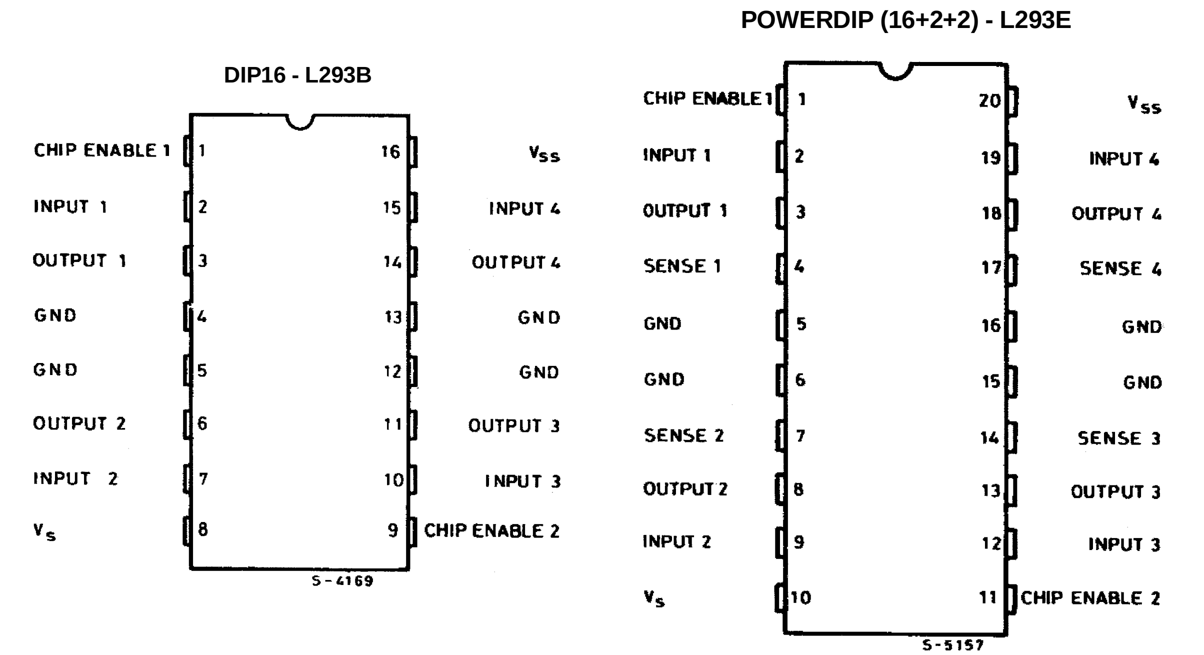
DESCRIPTION

The L293B and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

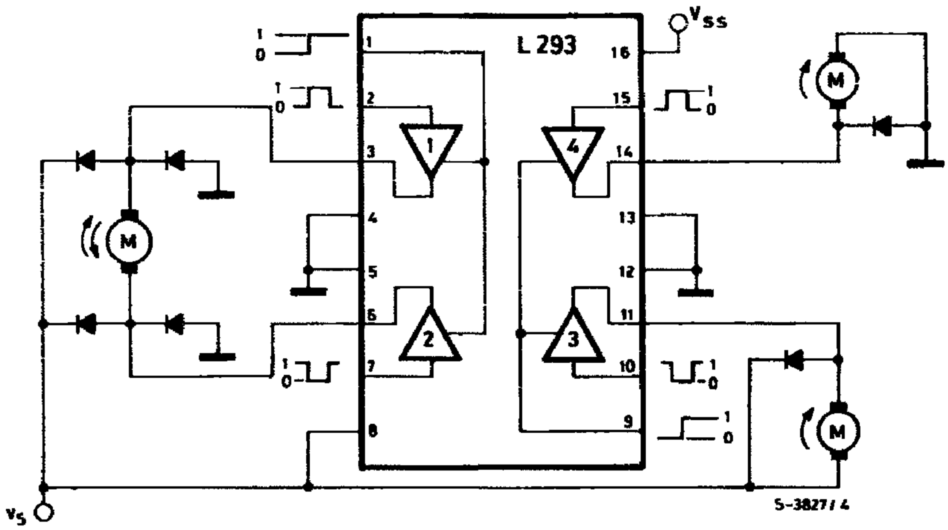
The L293B and L293E are package in 16 and 20-pin plastic DIPs respectively ; both use the four center pins to conduct heat to the printed circuit board.

PIN CONNECTION (Top view)

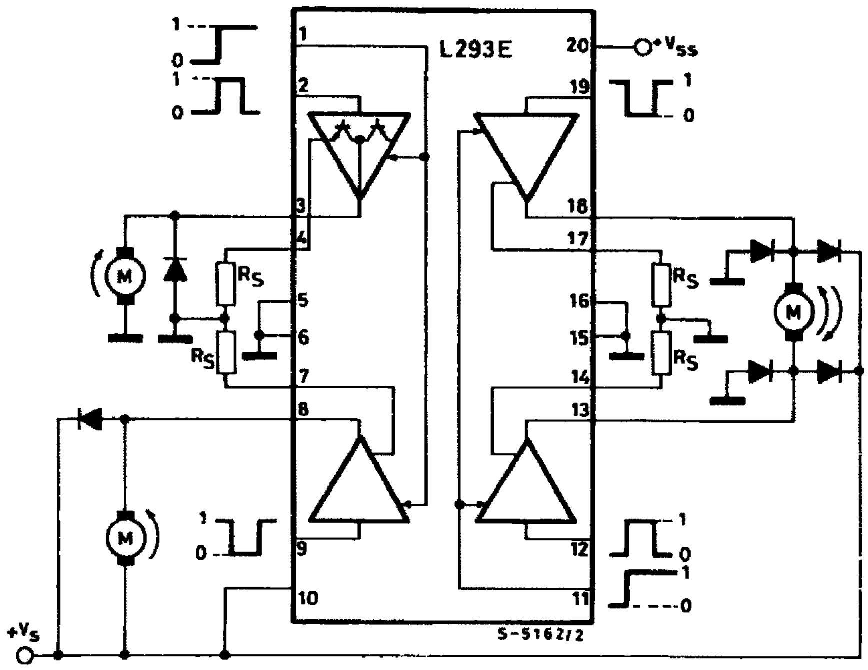


BLOCK DIAGRAMS

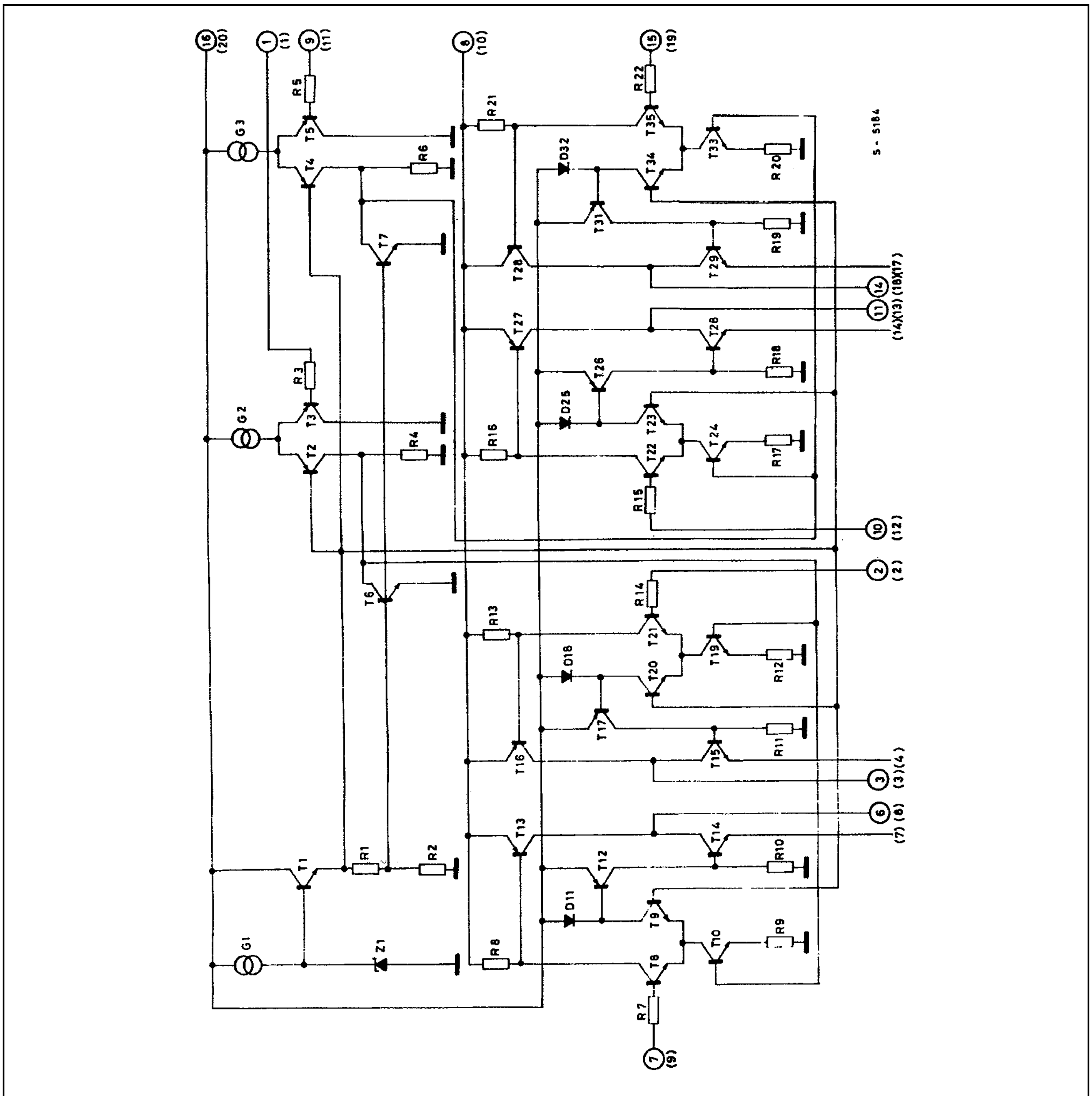
DIP16 - L293B



POWERDIP (16+2+2) - L293E



SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).
O Pins of L293 () Pins of L293E.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	36	V
V_{SS}	Logic Supply Voltage	36	V
V_i	Input Voltage	7	V
V_{inh}	Inhibit Voltage	7	V
I_{out}	Peak Output Current (non repetitive t = 5ms)	2	A
P_{tot}	Total Power Dissipation at $T_{ground\text{-}pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and Junction Temperature	–40 to +150	^oC

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

ELECTRICAL CHARACTERISTCS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		V_{SS}		36	V
V_{SS}	Logic Supply Voltage		4.5		36	V
I_S	Total Quiescent Supply Current	V_i = L; I_o = 0; V_{inh} = H		2	6	mA
		V_i = h; I_o = 0; V_{inh} = H		16	24	mA
		V_{inh} = L			4	mA
I_{SS}	Total Quiescent Logic Supply Current	V_i = L; I_o = 0; V_{inh} = H		44	60	mA
		V_i = h; I_o = 0; V_{inh} = H		16	22	mA
		V_{inh} = L		16	24	mA
V_{iL}	Input Low Voltage		-0.3		1.5	V
V_{iH}	Input High Voltage	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		$V_{SS} > 7V$	2.3		7	V
I_{iL}	Low Voltage Input Current	V_{il} = 1.5V			-10	µA
I_{iH}	High Voltage Input Current	$2.3V \leq V_{IH} \leq V_{SS} - 0.6V$		30	100	µA
V_{inhL}	Inhibit Low Voltage		-0.3		1.5	V
V_{inhH}	Inhibit High Voltage	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		$V_{SS} > 7V$	2.3		7	V
I_{inhL}	Low Voltage Inhibit Current	V_{inhL} = 1.5V		-30	-100	µA
I_{inhH}	High Voltage Inhibit Current	$2.3V \leq V_{inhH} \leq Vss - 0.6V$			±10	µA
V_{CEsatH}	Source Output Saturation Voltage	I_o = -1A		1.4	1.8	V
V_{CEsatL}	Sink Output Saturation Voltage	I_o = 1A		1.2	1.8	V
V_{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)				2	V
t_r	Rise Time	0.1 to 0.9 V_o (*)		250		ns
t_f	Fall Time	0.9 to 0.1 V_o (*)		250		ns
t_{on}	Turn-on Delay	0.5 V_i to 0.5 V_o (*)		750		ns
t_{off}	Turn-off Delay	0.5 V_i to 0.5 V_o (*)		200		ns

* See figure 1
** Referred to L293E

TRUTH TABLE

V_i (each channel)	V_o	V_{inh} (**)
H	H	H
L	L	H
H	X (*)	L
L	X (*)	L

(*) High output impedance
(**) Relative to the considerate channel

Figure 1. Switching Timers

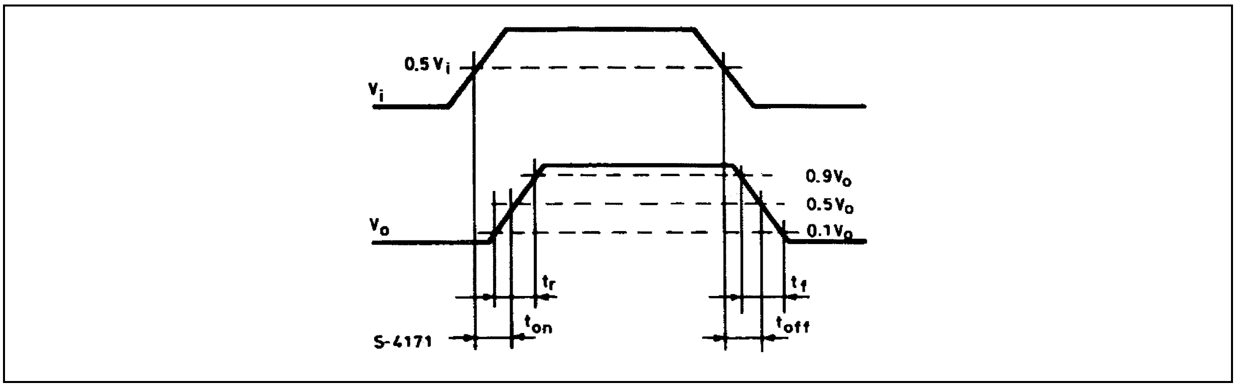


Figure 2. Saturation voltage versus Output Current

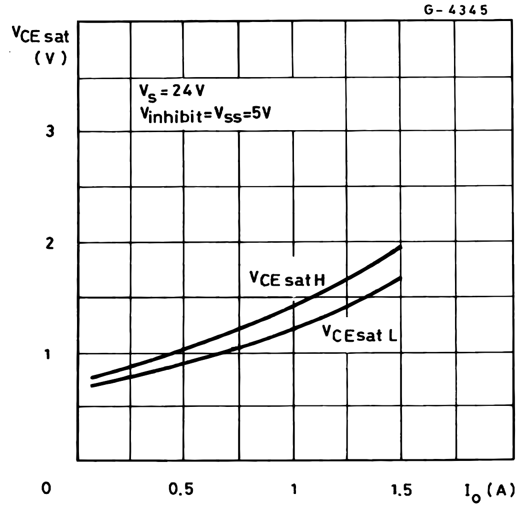


Figure 4. Sink Saturation Voltage versus Ambient Temperature

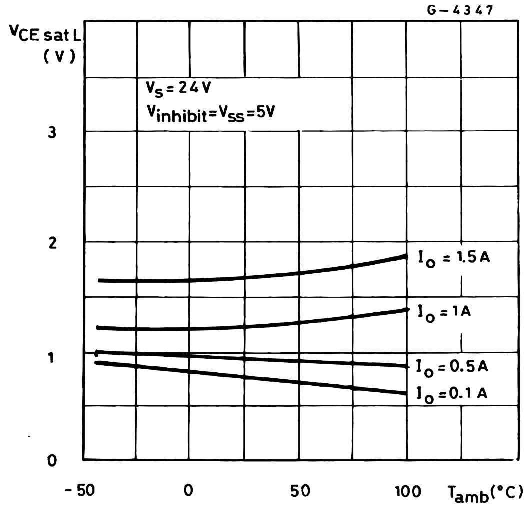


Figure 3. Source Saturation Voltage versus Ambient Temperature

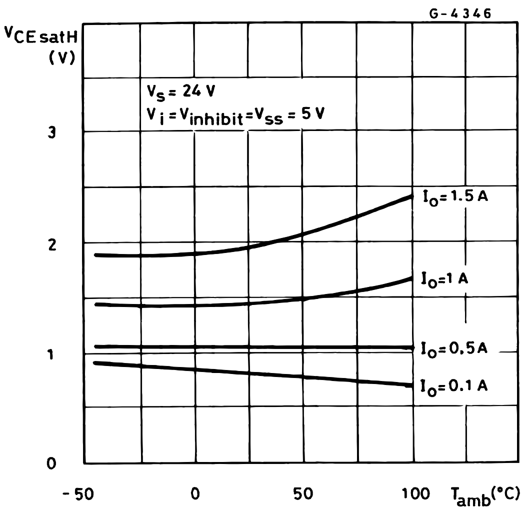


Figure 5. Quiescent Logic Supply Current versus Logic Supply Voltage

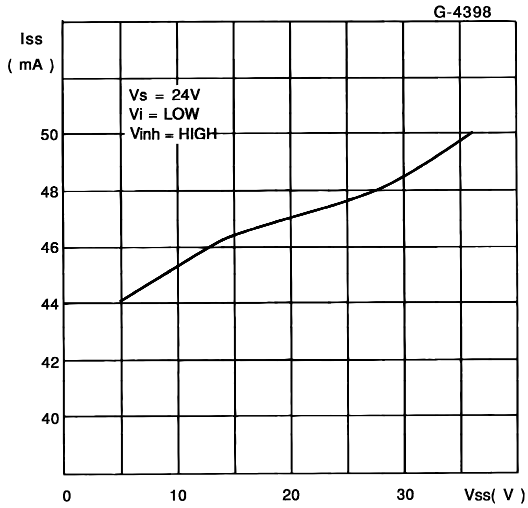


Figure 6. Output Voltage versus Input Voltage

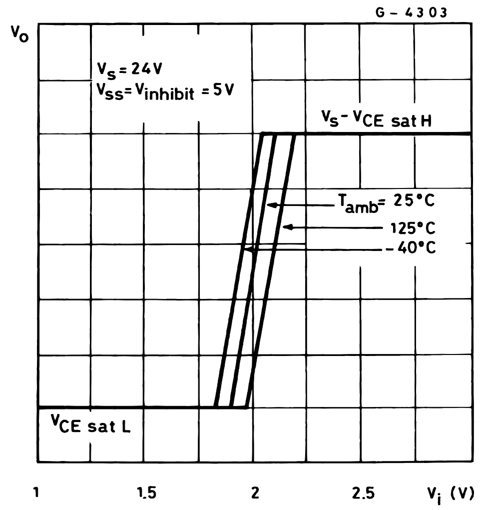
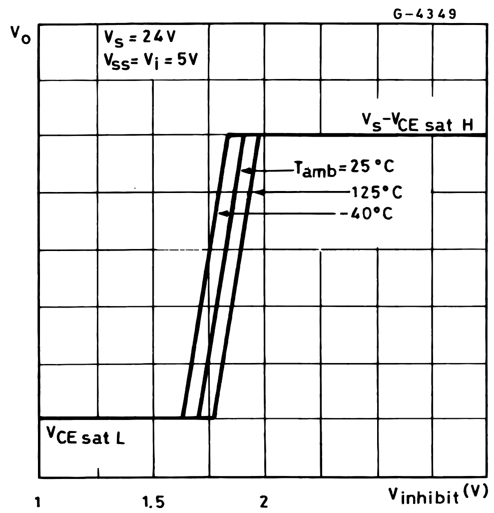
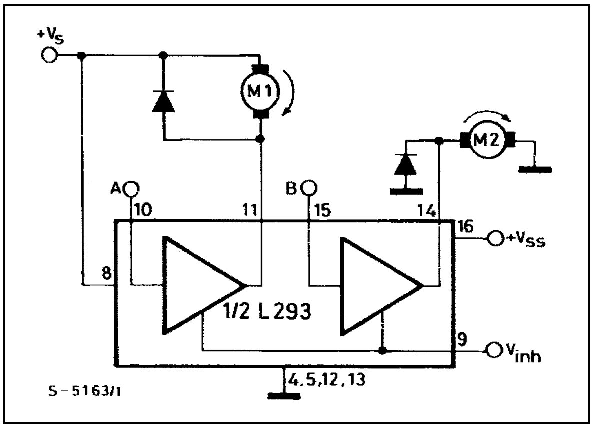


Figure 7. Output Voltage versus Inhibit Voltage



APPLICATION INFORMATION

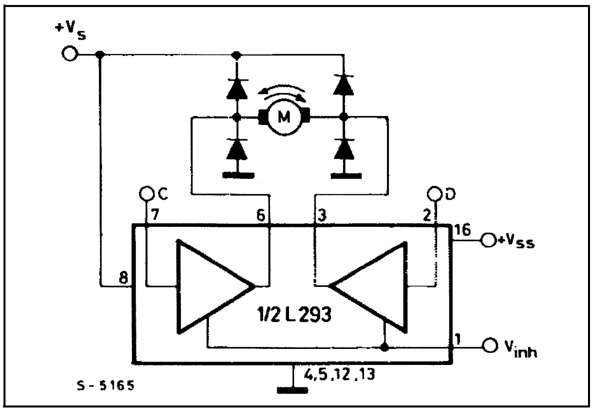
Figure 8. DC Motor Controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running	X	Free Running
		Motor Stop		Motor Stop

L = Low H = High X = Don't Care

Figure 9. Bidirectional DC Motor Control



Inputs	Function	
V_{inh} = H	C = H ; D = L	Turn Right
	C = L ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{inh} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't Care

Figure 10. Bipolar Stepping Motor Control

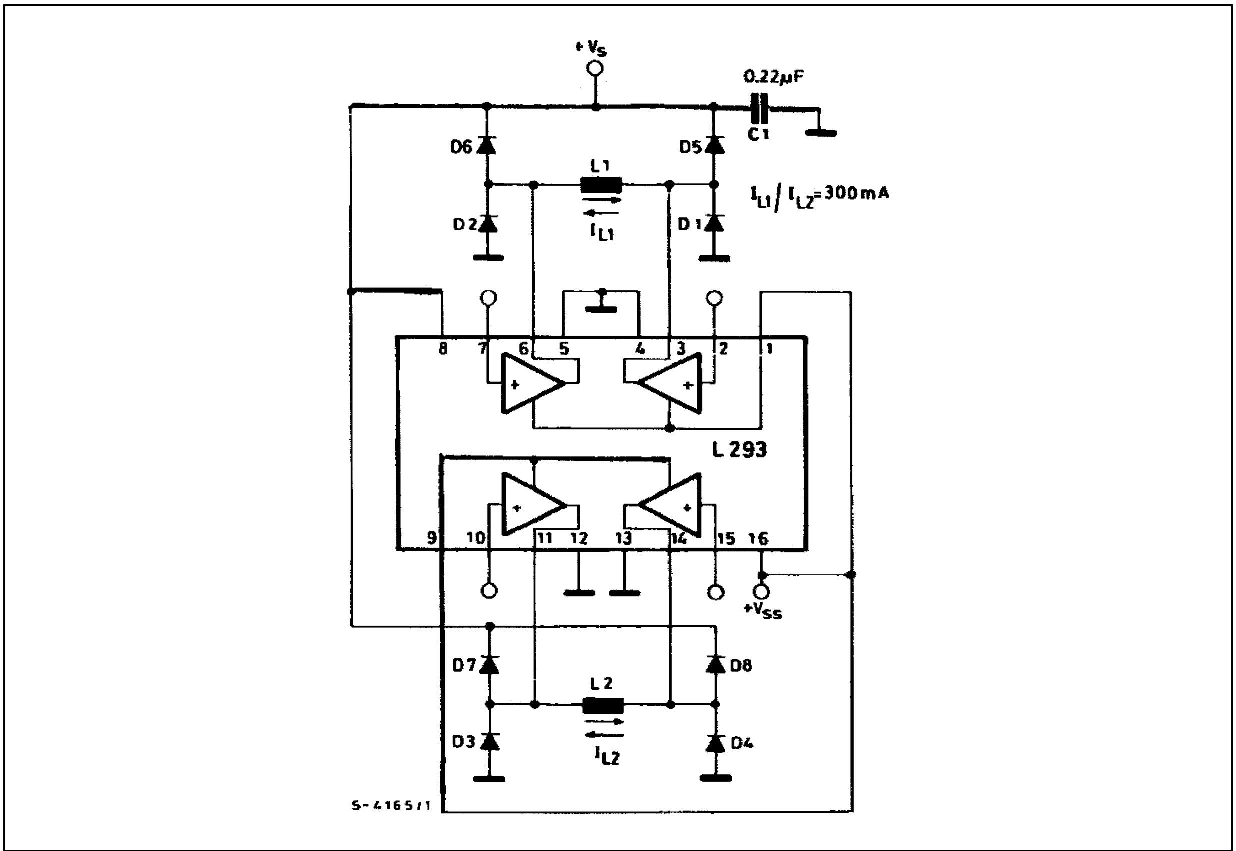
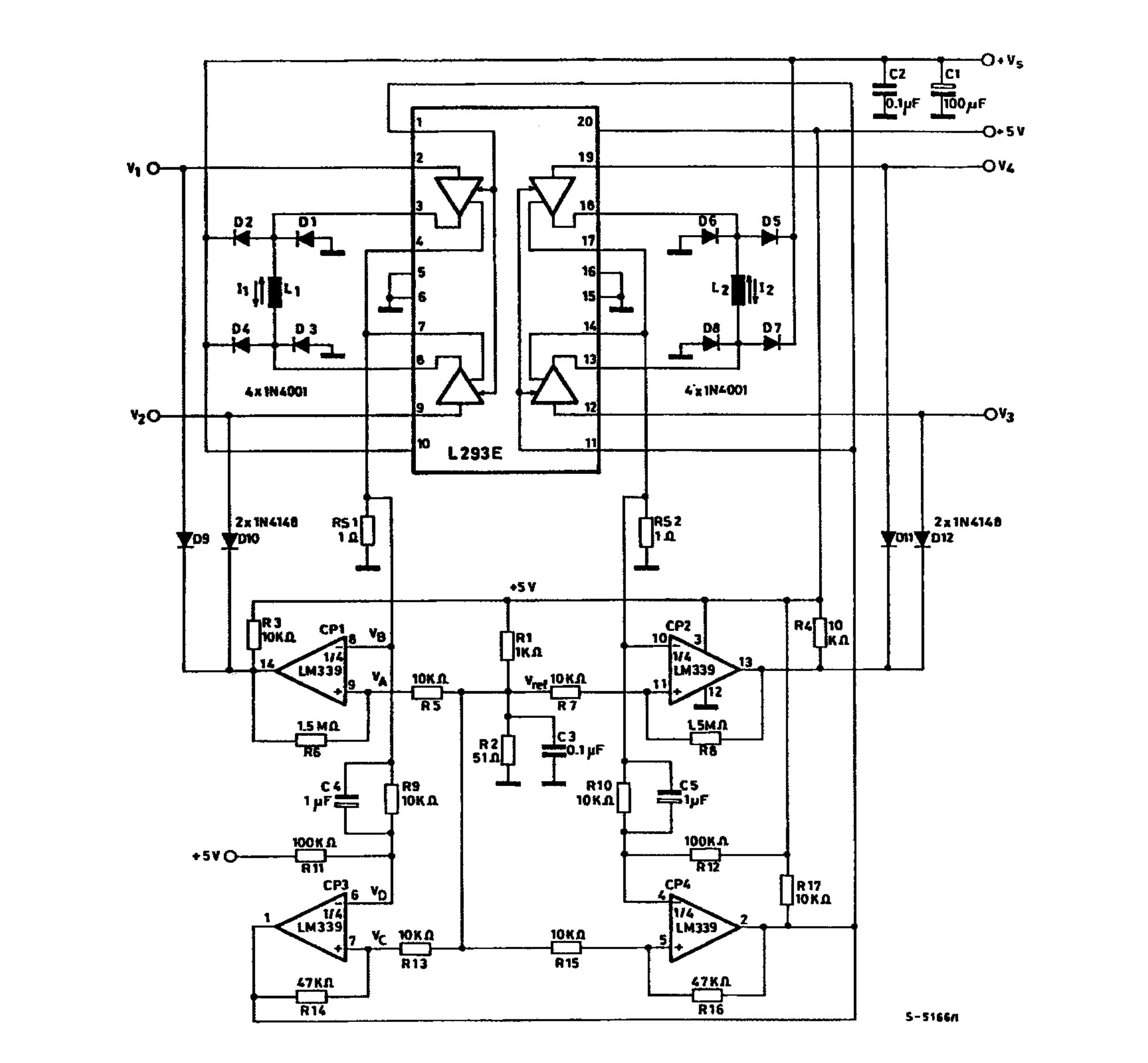


Figure 11. Stepping Motor Driver with Phase Current Control and Short Circuit Protection



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L293B and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12. Example of P.C. Board Copper Area which is Used as Heatsink

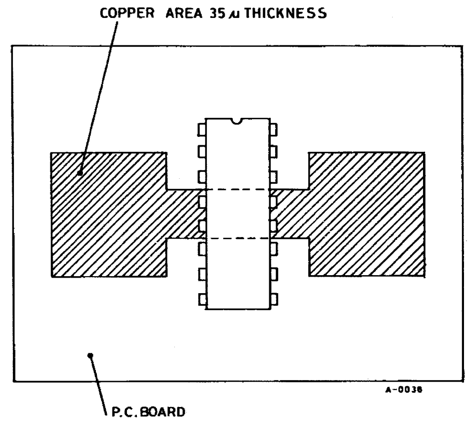
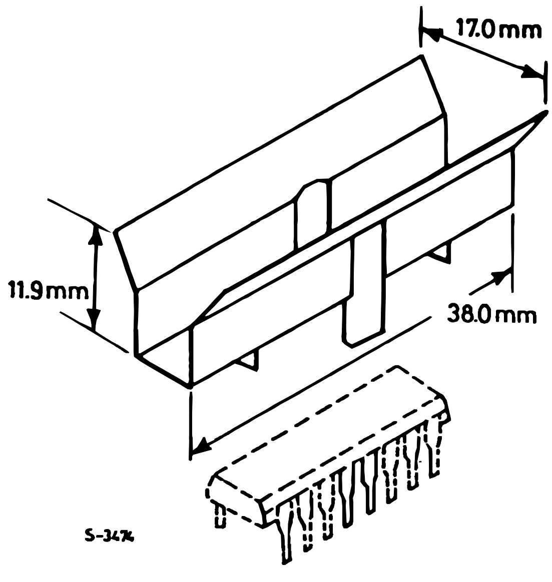
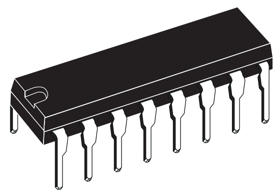


Figure 13. External Heatsink Mounting Example (R_{th} = 30°C/W)

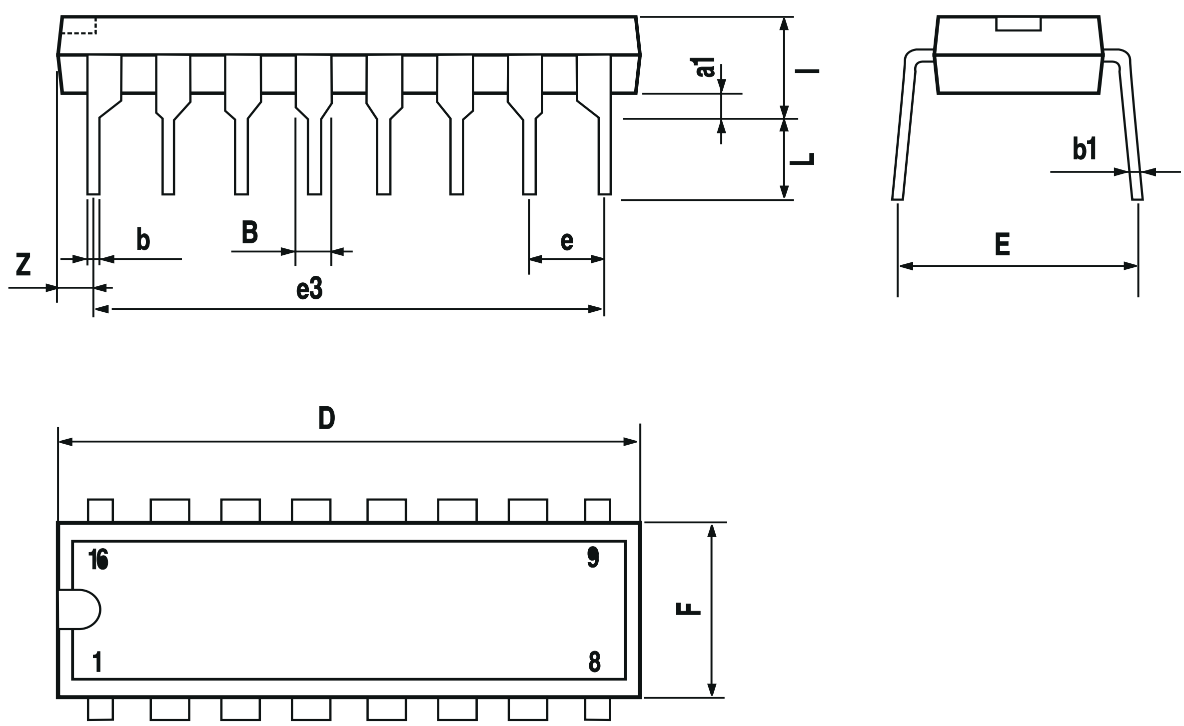


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

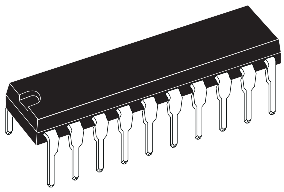


DIP16

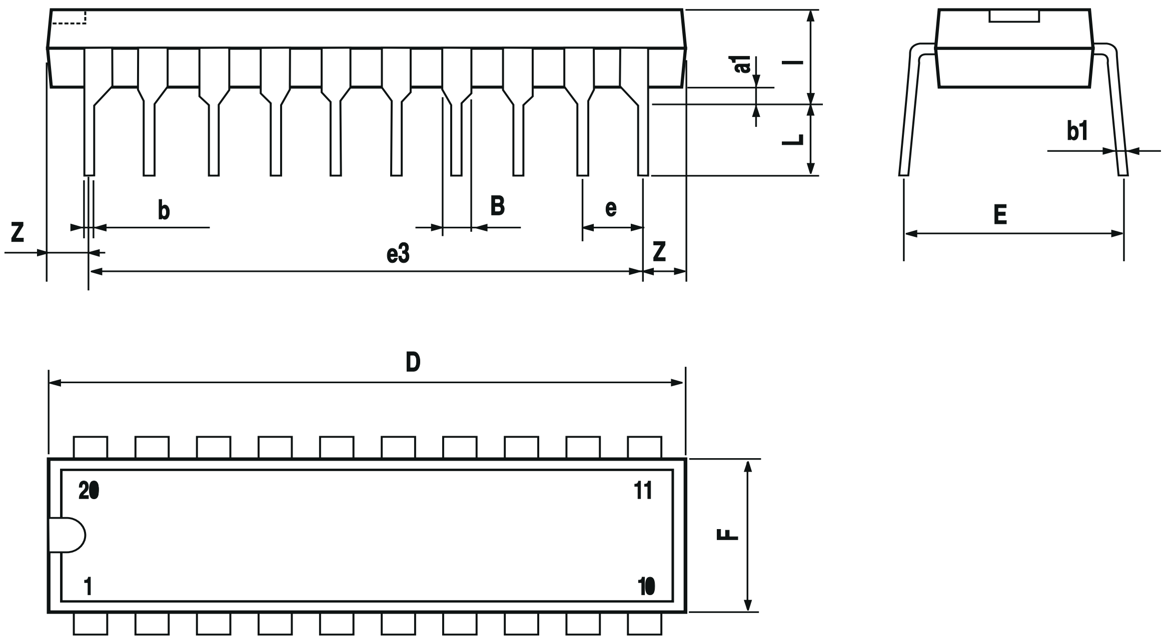


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



Powerdip 20



National Semiconductor

May 2000

LM78XX
Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

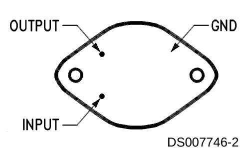
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

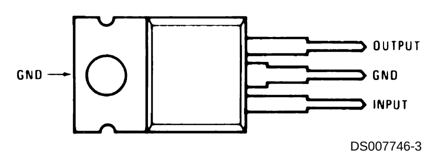
Connection Diagrams

Metal Can Package
TO-3 (K)
Aluminum



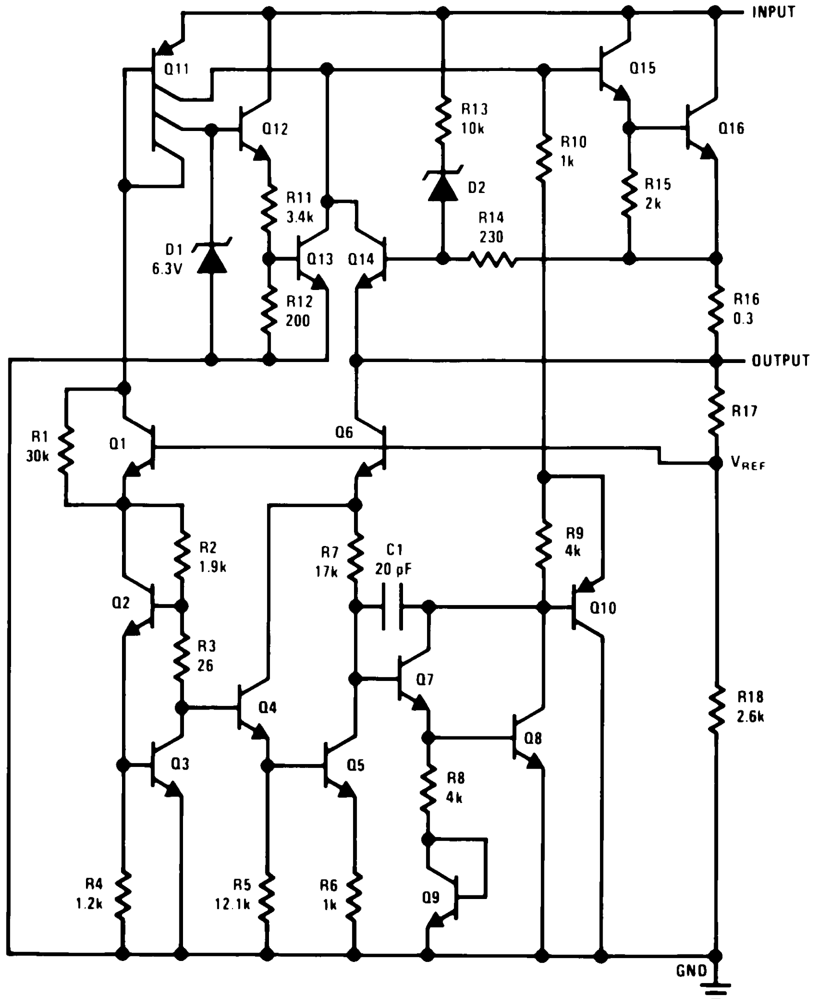
Bottom View
Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



Top View
Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

Schematic



DS007746-1

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	
(V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0˚C to +70˚C
Maximum Junction Temperature	
(K Package)	150˚C
(T Package)	150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300˚C
TO-220 Package T	230˚C

Electrical Characteristics LM78XXC (Note 2)

0˚C ≤ T_J ≤ 125˚C unless otherwise noted.

		Output Voltage		5V			12V			15V			Units
		Input Voltage (unless otherwise noted)		10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25˚C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)		V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25˚C		3	50		4	120		4	150	mV
			ΔV_{IN}		(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)		V
			0˚C ≤ Tj ≤ +125˚C			50			120			150	mV
			ΔV_{IN}		(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)		V
		I_O ≤ 1A	Tj = 25˚C			50			120			150	mV
			ΔV_{IN}		(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)		V
			0˚C ≤ Tj ≤ +125˚C			25			60			75	mV
			ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)		V
ΔV_O	Load Regulation	Tj = 25˚C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0˚C ≤ Tj ≤ +125˚C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25˚C			8			8			8	mA
			0˚C ≤ Tj ≤ +125˚C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25˚C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN}≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		I_O ≤ 500 mA, 0˚C ≤ Tj ≤ +125˚C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN}≤ 30)			(17.5 ≤ V_{IN} ≤ 30)		V
V_N	Output Noise Voltage	T_A =25˚C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25˚C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0˚C ≤ Tj ≤ +125˚C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		V
R_O	Dropout Voltage	Tj = 25˚C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ

Electrical Characteristics LM78XXC (Note 2) (Continued)

0˚C ≤ T_J ≤ 125˚C unless otherwise noted.

Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			**10V**			**19V**			**23V**			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
	Short-Circuit Current	Tj = 25˚C		2.1			1.5			1.2		A
	Peak Output Current	Tj = 25˚C		2.4			2.4			2.4		A
	Average TC of V_{OUT}	0˚C ≤ Tj ≤ +125˚C, I_O = 5 mA		0.6			1.5			1.8		mV/˚C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25˚C, I_O ≤ 1A		7.5		14.6			17.7			V

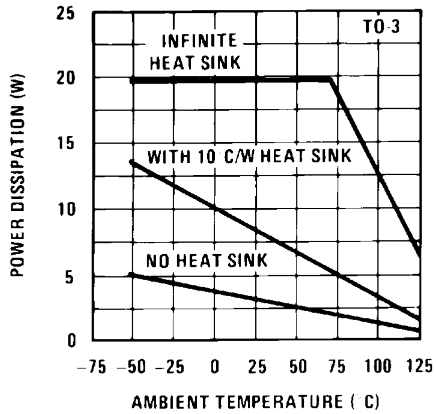
Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4˚C/W junction to case and 35˚C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4˚C/W junction to case and 50˚C/W case to ambient.

Note 2: All characteristics are measured with capacitor across the input of 0.22 µF, and a capacitor across the output of 0.1µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and the test conditions, see Electrical Characteristics.

Typical Performance Characteristics

Maximum Average Power Dissipation



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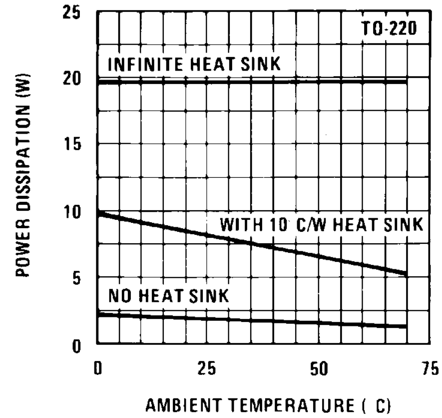
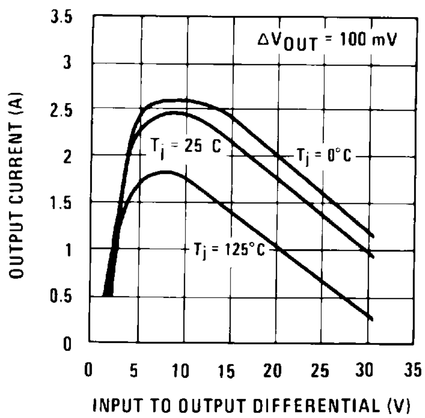
Maximum Average Power Dissipation



DS007746-6

Peak Output Current



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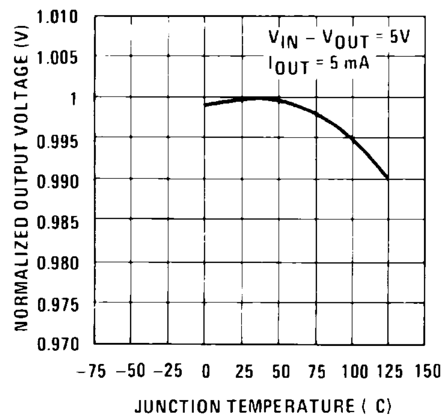
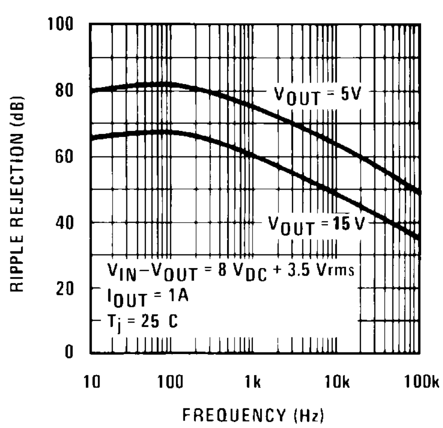
Output Voltage (Normalized to 1V at T_J = 25°C)



DS007746-8

Ripple Rejection



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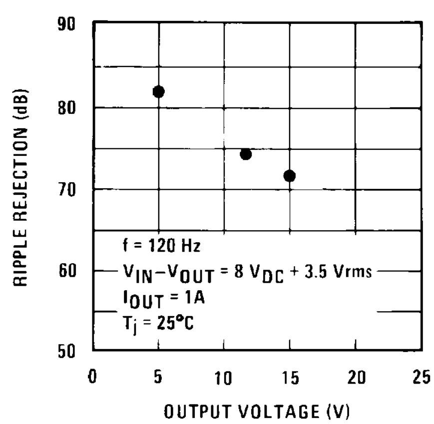
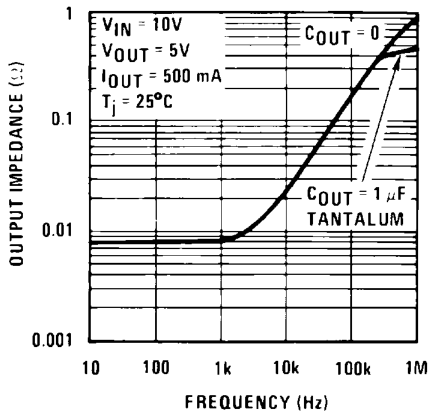
Ripple Rejection



DS007746-10

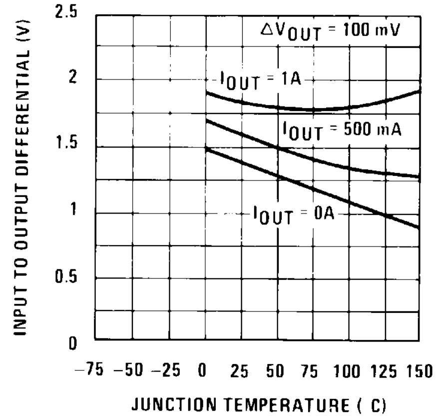
Typical Performance Characteristics (Continued)

Output Impedance



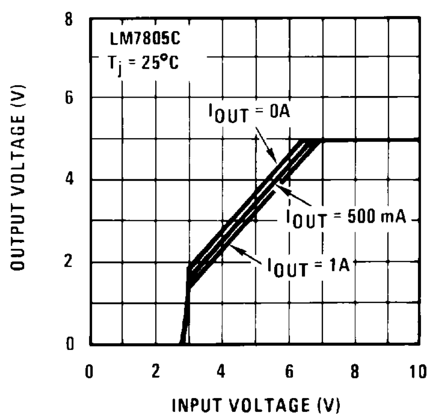
DS007746-11

Dropout Voltage



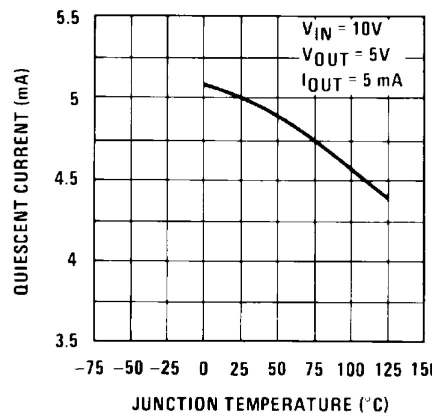
DS007746-12

Dropout Characteristics



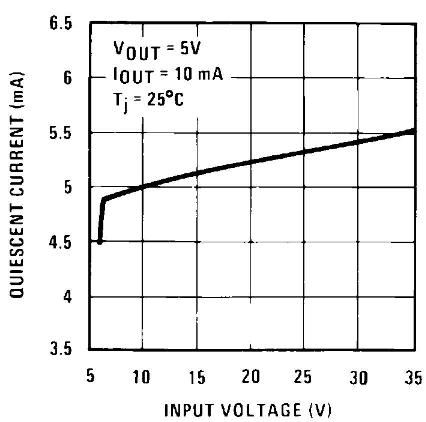
DS007746-13

Quiescent Current



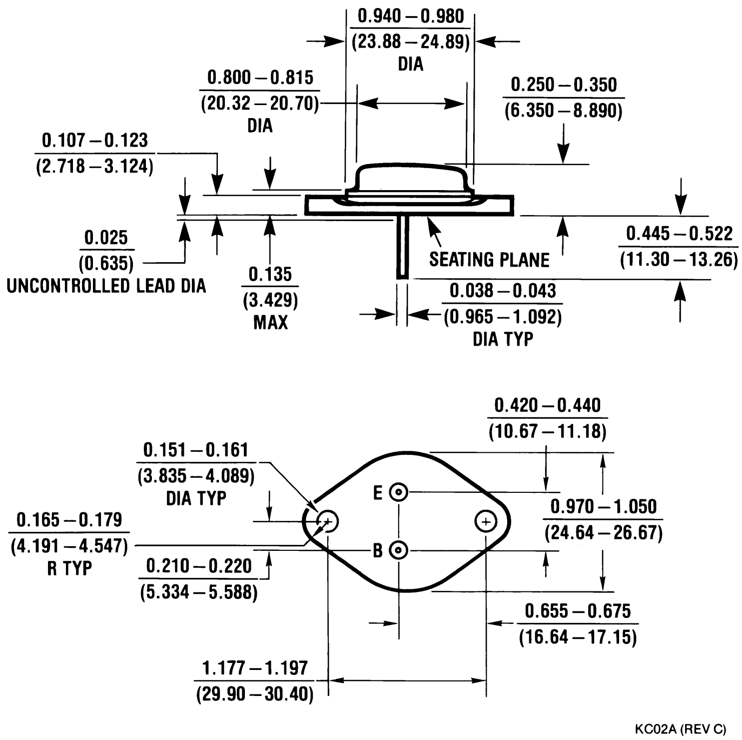
DS007746-14

Quiescent Current



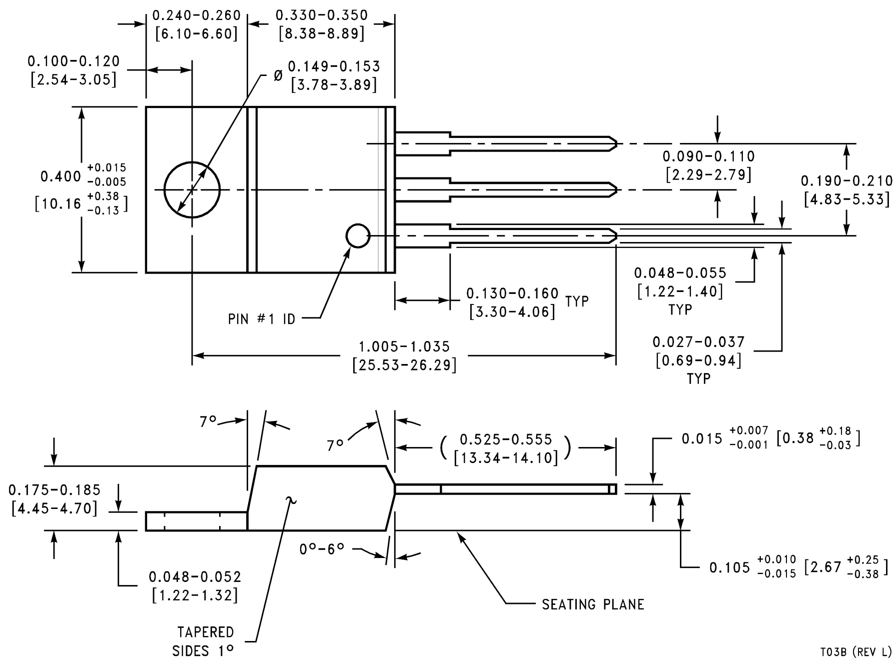
DS007746-15

Physical Dimensions inches (millimeters) unless otherwise noted



Aluminum Metal Can Package (KC)
Order Number LM7805CK, LM7812CK or LM7815CK
NS Package Number KC02A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-220 Package (T)
Order Number LM7805CT, LM7812CT or LM7815CT
NS Package Number T03B

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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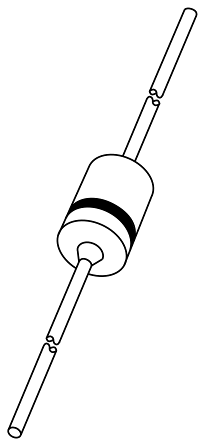
DISCRETE SEMICONDUCTORS

DATA SHEET



1N4148; 1N4448
High-speed diodes

Product specification
Supersedes data of 1999 May 25

2002 Jan 23

Philips
Semiconductors

PHILIPS

FEATURES

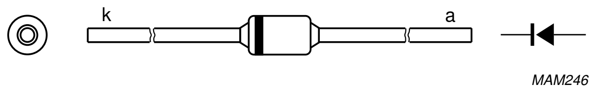
- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 100 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

- High-speed switching.

DESCRIPTION

The 1N4148 and 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.



The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	100	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	non-repetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 µs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	see Fig.3			
	1N4148	I_F = 10 mA	–	1	V
	1N4448	I_F = 5 mA	0.62	0.72	V
		I_F = 100 mA	–	1	V
I_R	reverse current	V_R = 20 V; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	–	50	μA
I_R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	–	3	μA
C_d	diode capacitance	f = 1 MHz; V_R = 0; see Fig.6	–	4	pF
t_{rr}	reverse recovery time	when switched from I_F = 10 mA to I_R = 60 mA; R_L = 100 Ω; measured at I_R = 1 mA; see Fig.7	–	4	ns
V_{fr}	forward recovery voltage	when switched from I_F = 50 mA; t_r = 20 ns; see Fig.8	–	2.5	V

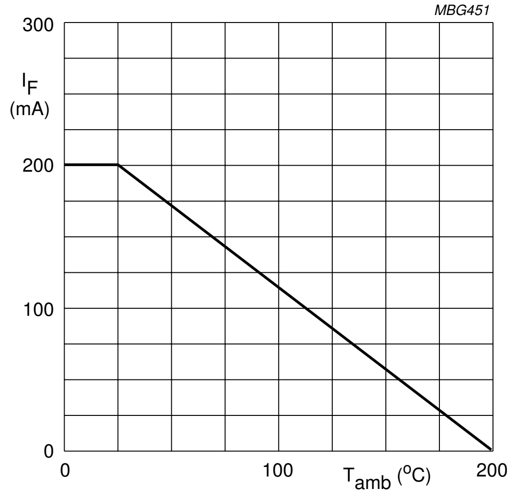
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

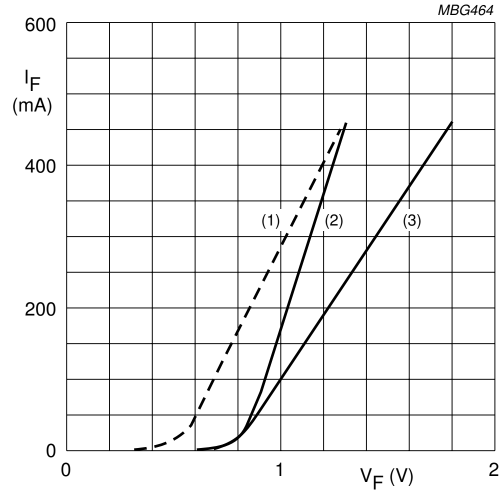
1. Device mounted on a printed circuit-board without metallization pad.

GRAPHICAL DATA



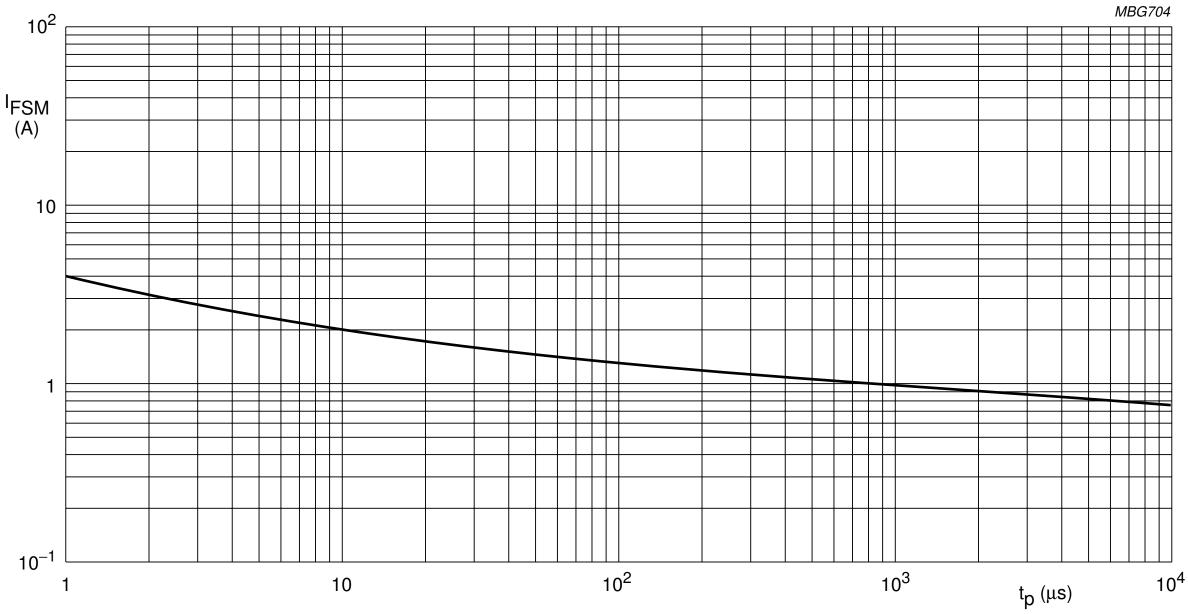
Device mounted on an FR4 printed-circuit board; lead length 10 mm.

Fig.2 Maximum permissible continuous forward current as a function of ambient temperature.



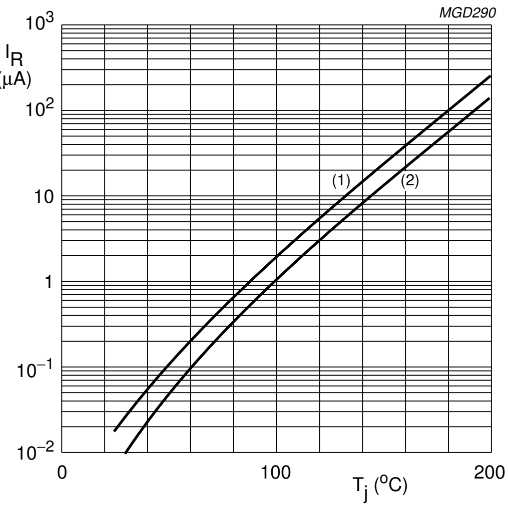
(1) T_j = 175 °C; typical values.
(2) T_j = 25 °C; typical values.
(3) T_j = 25 °C; maximum values.

Fig.3 Forward current as a function of forward voltage.



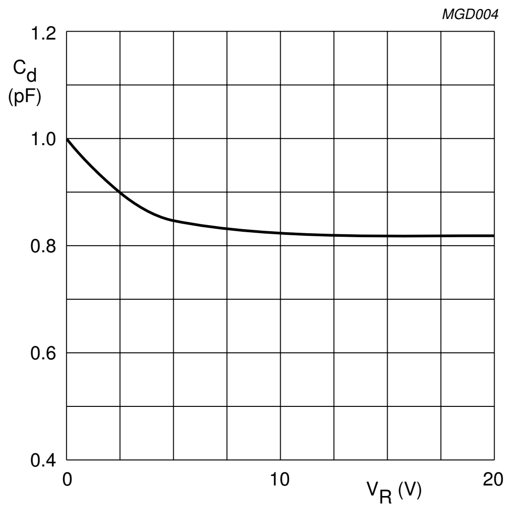
Based on square wave currents.
T_j = 25 °C prior to surge.

Fig.4 Maximum permissible non-repetitive peak forward current as a function of pulse duration.



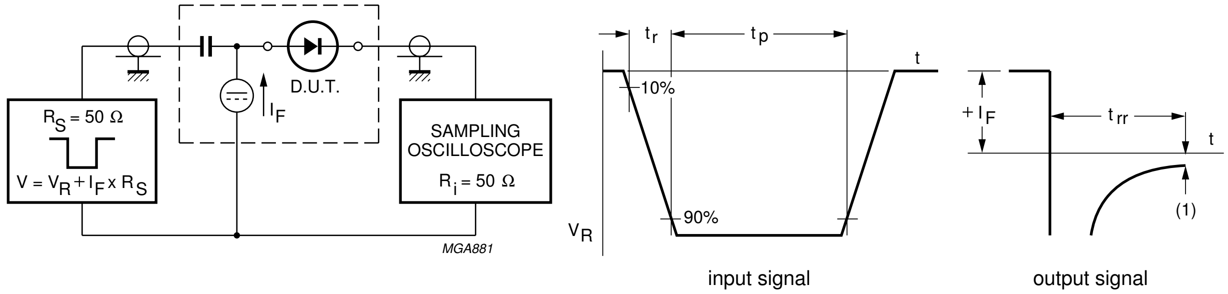
(1) V_R = 75 V; typical values.
(2) V_R = 20 V; typical values.

Fig.5 Reverse current as a function of junction temperature.



f = 1 MHz; T_j = 25 °C.

Fig.6 Diode capacitance as a function of reverse voltage; typical values.



(1) I_R = 1 mA.

Fig.7 Reverse recovery voltage test circuit and waveforms.

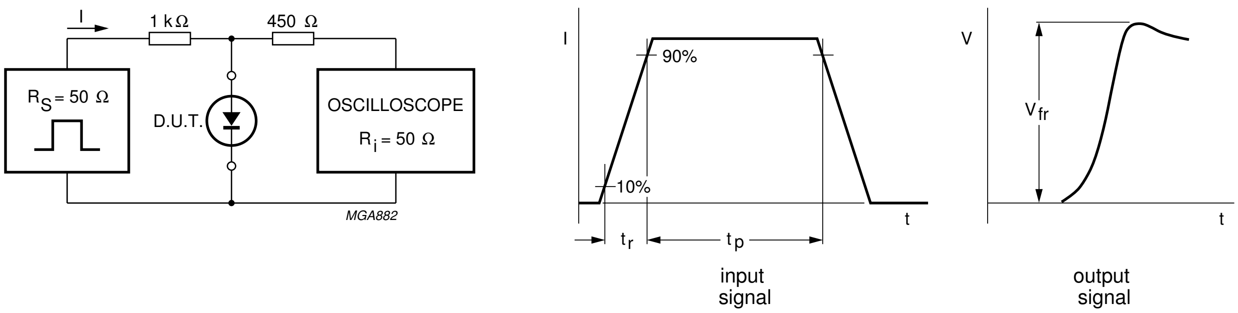
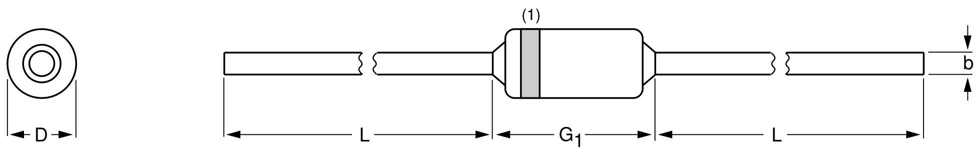


Fig.8 Forward recovery voltage test circuit and waveforms.

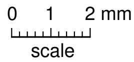
PACKAGE OUTLINE

Hermetically sealed glass package; axial leaded; 2 leads **SOD27**



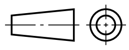
DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G_1 max.	L min.
mm	0.56	1.85	4.25	25.4



Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD27	A24	DO-35	SC-40			97-06-09

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA74

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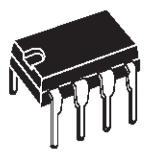
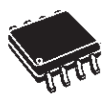
NE555
SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER^{o}C



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

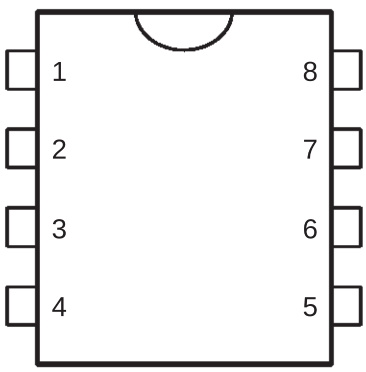
DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

ORDER CODES

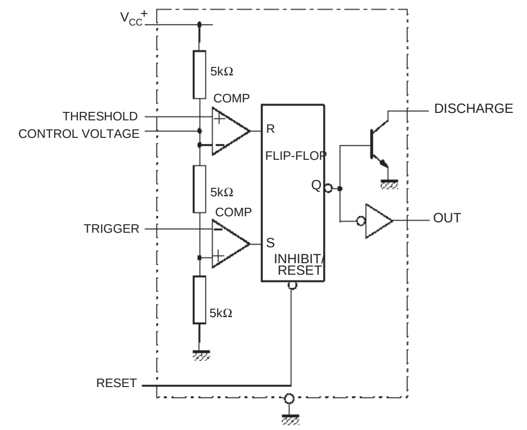
Part Number	Temperature Range	Package	
		N	D
NE555	0^{o}C, 70^{o}C	•	•
SA555	–40^{o}C, 105^{o}C	•	•
SE555	–55^{o}C, 125^{o}C	•	•

PIN CONNECTIONS (top view)

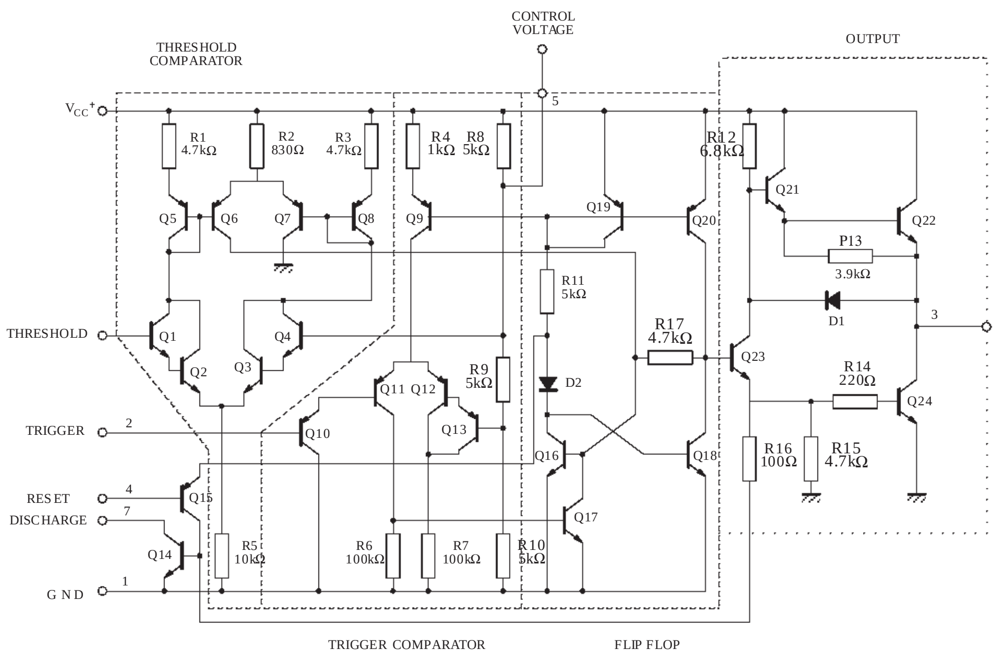


1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage		18	V
T_{oper}	Operating Free Air Temperature Range	for NE555 for SA555 for SE555	0 to 70 –40 to 105 –55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) (- note 1) Low State V_{CC} = +5V V_{CC} = +15V High State V_{CC} = 5V		 3 10 2	 5 12		 3 10 2	 6 15	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2 100 0.2		 1 50 0.1	 3 0.5	 % ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15			 2.25 150 0.3		 % ppm/°C %/V
V_{CL}	Control Voltage level V_{CC} = +15V V_{CC} = +5V	 9.6 2.9	 10 3.33	 10.4 3.8	 9 2.6	 10 3.33	 11 4	V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 9.4 2.7	 10 3.33	 10.6 4	 8.8 2.4	 10 3.33	 11.2 4.2	V
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.8 1.45	 5 1.67	 5.2 1.9	 4.5 1.1	 5 1.67	 5.6 2.2	V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V		 0.1 0.4	 0.4 1		 0.1 0.4	 0.4 1.5	mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V, $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V, $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage V_{CC} = +15V, $I_{O(source)}$ = 200mA $I_{O(source)}$ = 100mA V_{CC} = +5V, $I_{O(source)}$ = 100mA	 13 3	 12.5 13.3 3.3		 12.75 2.75	 12.5 13.3 3.3		V

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering

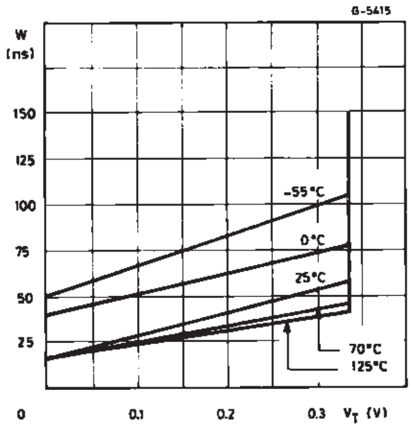


Figure 2 : Supply Current versus Supply Voltage

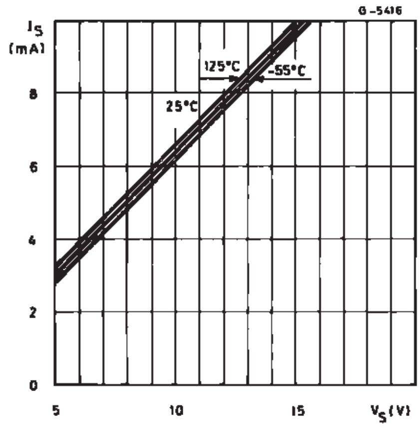


Figure 3 : Delay Time versus Temperature

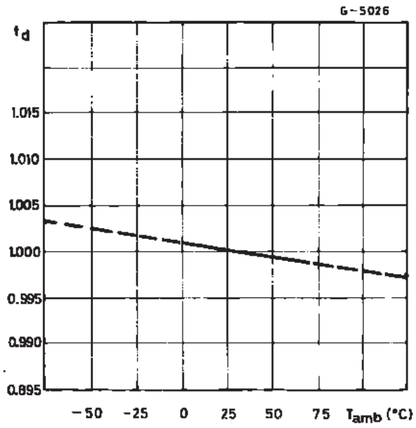


Figure 4 : Low Output Voltage versus Output Sink Current

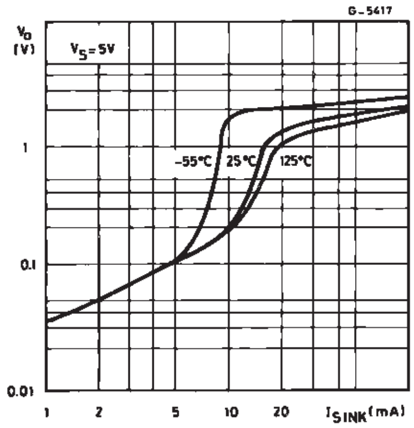


Figure 5 : Low Output Voltage versus Output Sink Current

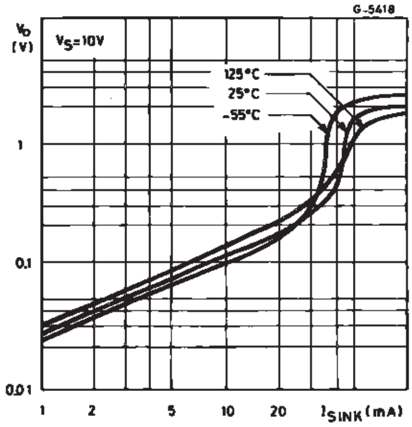


Figure 6 : Low Output Voltage versus Output Sink Current

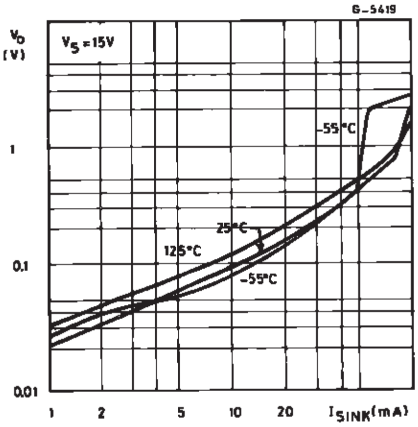


Figure 7 : High Output Voltage Drop versus Output

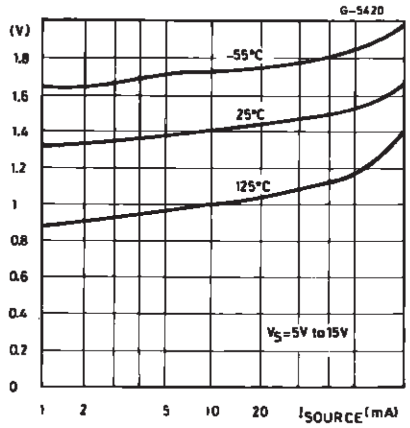


Figure 8 : Delay Time versus Supply Voltage

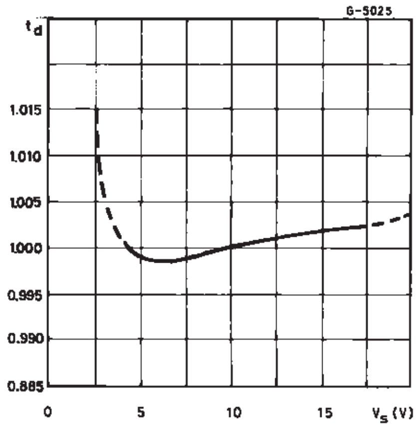
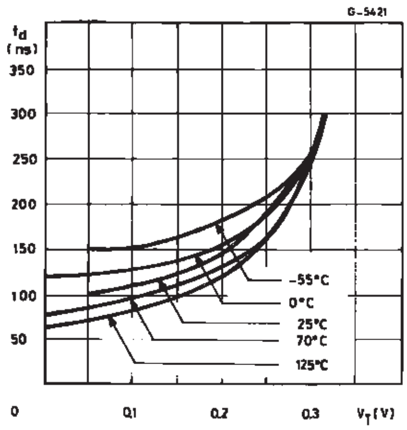


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value

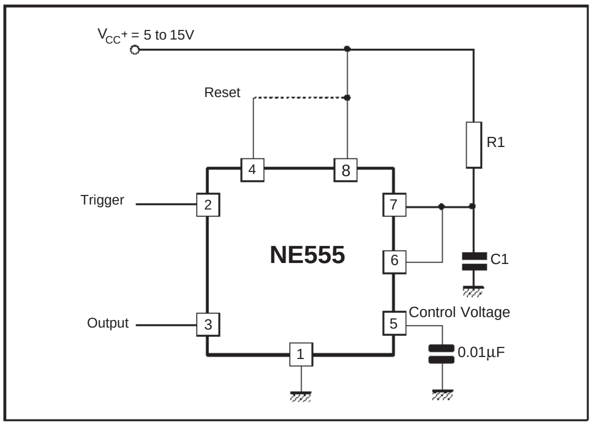


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R_1C_1 and is easily determined by figure 12.

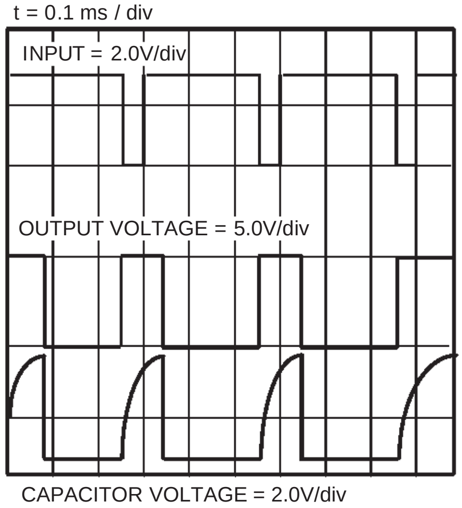
Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

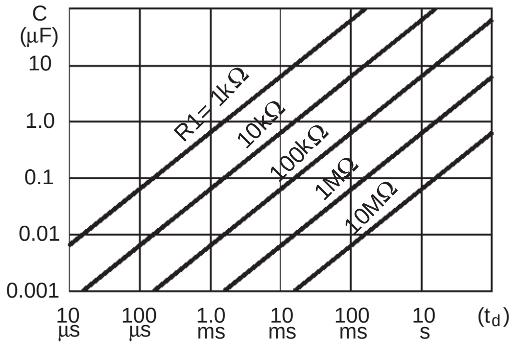
When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11



R1 = 9.1kΩ, C1 = 0.01µF, R_L = 1kΩ

Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{cc} and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

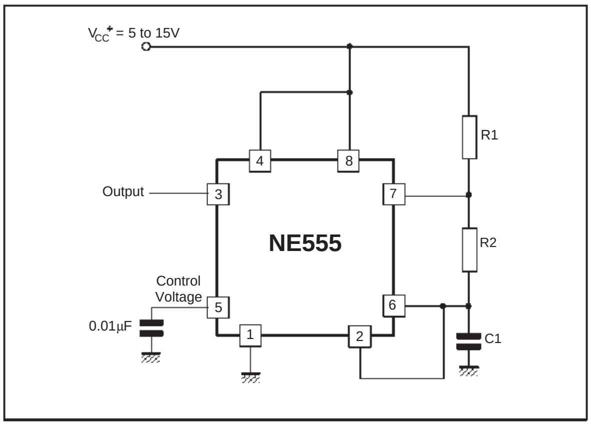


Figure 14 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t_1 = 0.693\ (R_1 + R_2)\ C_1$

and the discharge time (output LOW) by :

$t_2 = 0.693\ (R_2)\ C_1$

Thus the total period T is given by :

$T = t_1 + t_2 = 0.693\ (R_1 + 2R_2)\ C_1$

The frequency ofoscillation is them :

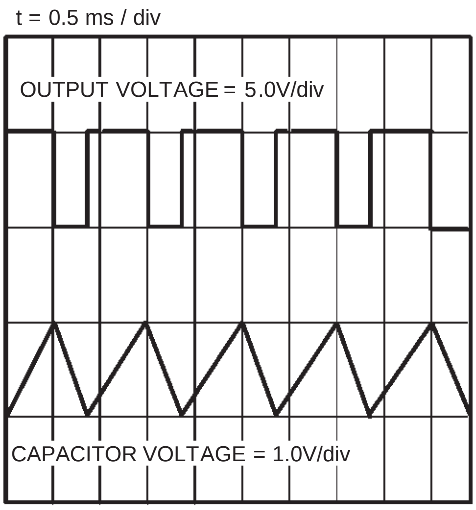
$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\ C_1}$$

and may be easily found by figure 15.

The duty cycle is given by :

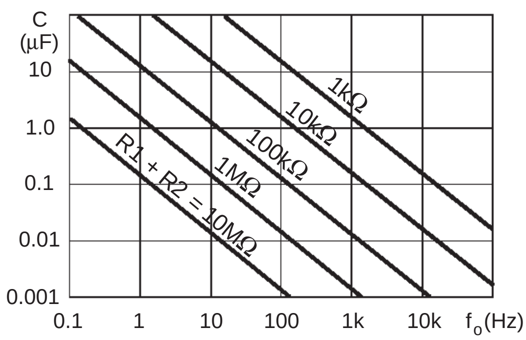
$$D = \frac{R_2}{R_1 + 2R_2}$$

Figure 14



$R1 = R2 = 4.8k\Omega$, $C1 = 0.1\mu F$, $R_L = 1k\Omega$

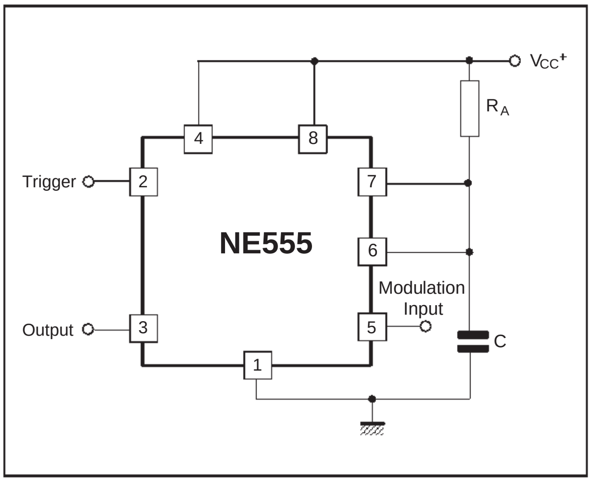
Figure 15 : Free Running Frequency versus R_1, R_2 and C_1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

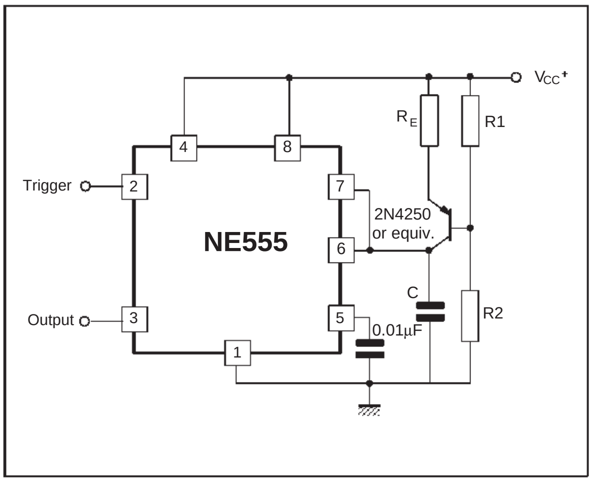
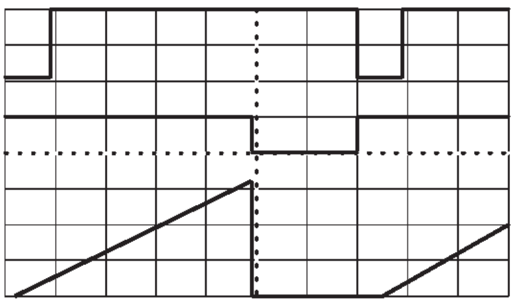


Figure 18 shows waveforms generator by the linear ramp.
The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



V_{CC} = 5V
Time = 20µs/DIV
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7kΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

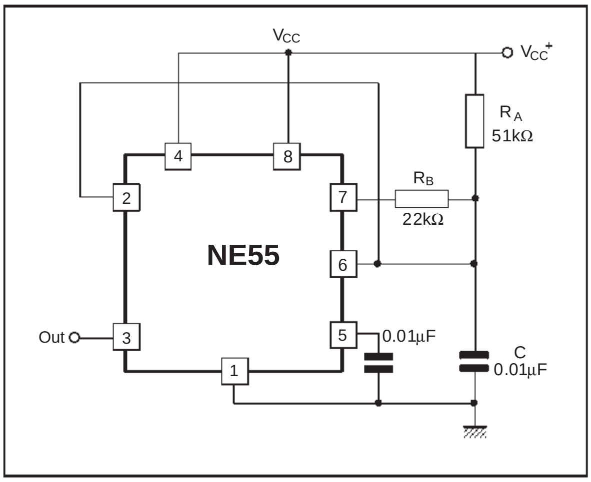
For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,
$t_1 = 0.693\ R_A\ C$.
For the output low it is t_2 =

$$[(R_A R_B)/(R_A + R_B)]\ CLn \left[\frac{R_B - 2R_A}{2R_B - R_A} \right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater

Figure 19 : 50% Duty Cycle Oscillator.

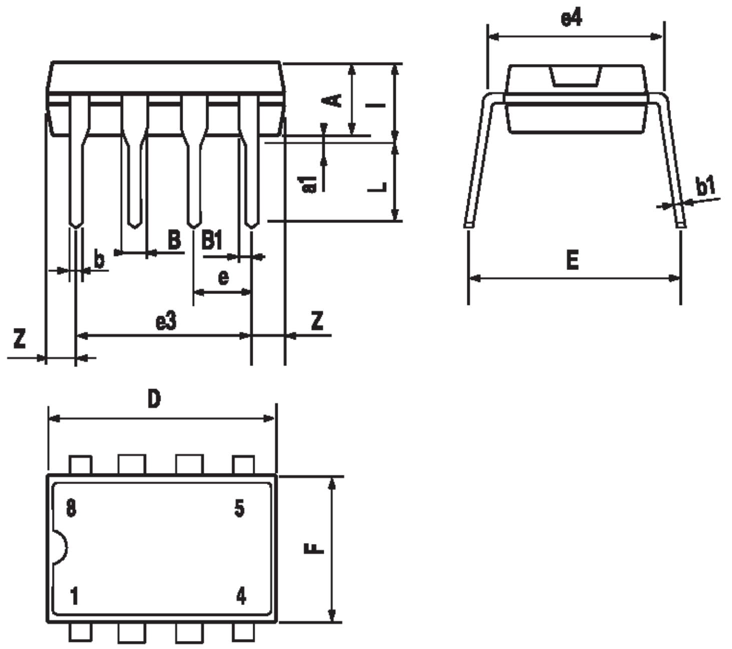


than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP

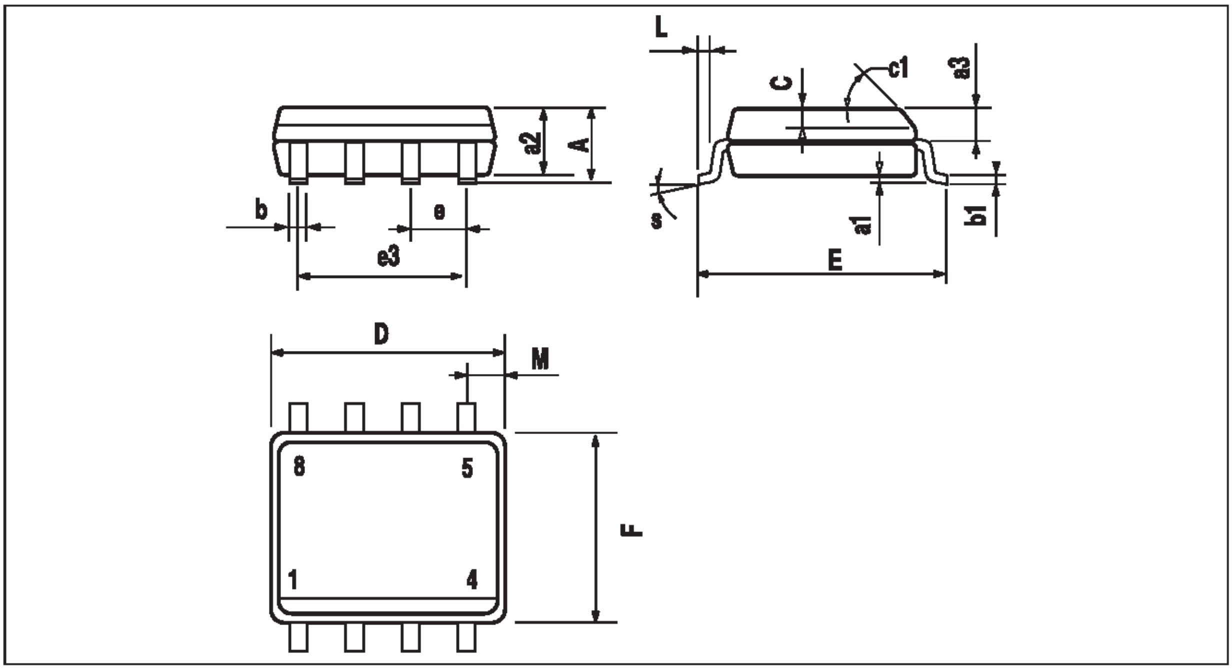


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45^{o} (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8^{o} (max.)					

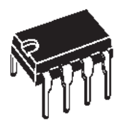
SO8.TBL

ORDER CODE :

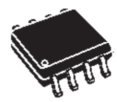
TL081
TL081A - TL081B

GENERAL PURPOSE J-FET SINGLE OPERATIONAL AMPLIFIERS

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The TL081, TL081A and TL081B are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

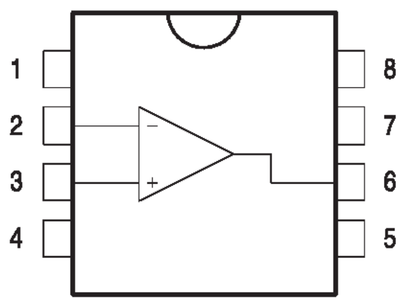
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
TL081M/AM/BM	-55°C, +125°C	•	•
TL081I/AI/BI	-40°C, +105°C	•	•
TL081C/AC/BC	0°C, +70°C	•	•
Example : TL081CD, TL081IN			

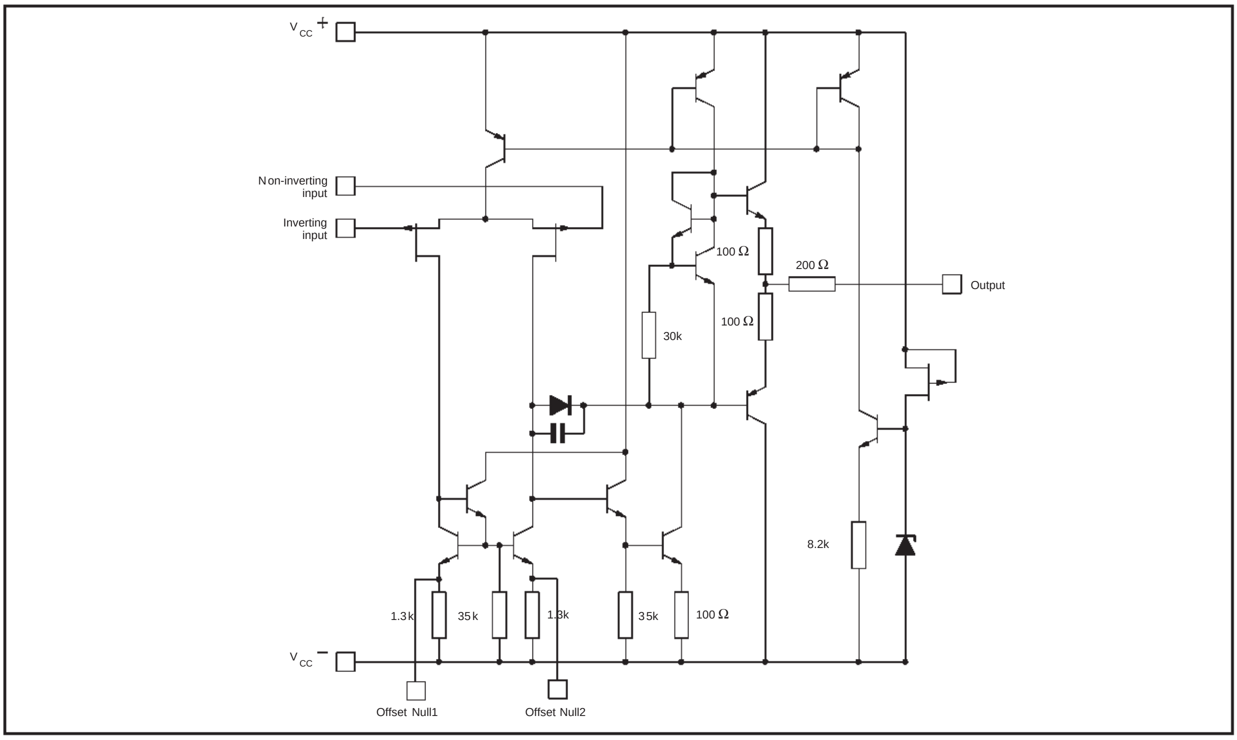
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)

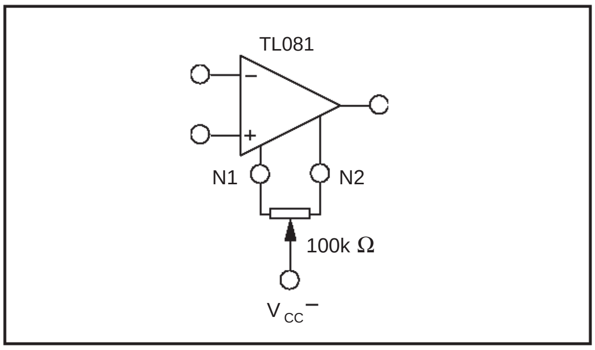


1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TL081M, AM, BM	TL081I, AI, BI	TL081C, AC, BC	Unit
V_{CC}	Supply voltage - note 1)	±18			V
V_i	Input Voltage - note 2)	±15			V
V_{id}	Differential Input Voltage - note 3)	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note 4)	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded

ELECTRICAL CHARACTERISTICS

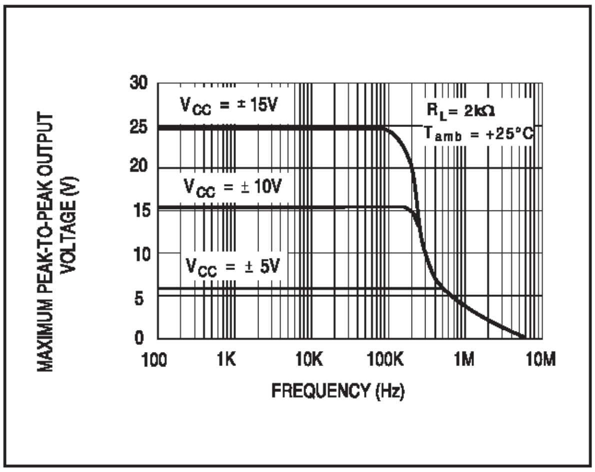
V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TL081I,M,AC,AI,AM, BC,BI,BM			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) T_{amb} = +25°C TL081 TL081A TL081B $T_{min} \le T_{amb} \le T_{max}$ TL081 TL081A TL081B		3 3 1	10 6 3 13 7 5		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current - note 1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 4		5	100 10	pA nA
I_{ib}	Input Bias Current -note 1 T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		20	200 20		20	400 20	nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_o = \pm10V$) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S = 50\Omega$) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{CC}	Supply Current, no load T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio ($R_S = 50\Omega$) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{os}	Output Short-circuit Current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = +25°C RL = 2kΩ RL = 10kΩ $T_{min} \le T_{amb} \le T_{max}$ RL = 2kΩ RL = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew Rate (T_{amb} = +25°C) V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain	8	16		8	16		V/µs
t_r	Rise Time (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		0.1			0.1		µs
K_{ov}	Overshoot (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		10			10		%
GBP	Gain Bandwidth Product (T_{amb} = +25°C) V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF, f= 100kHz	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω

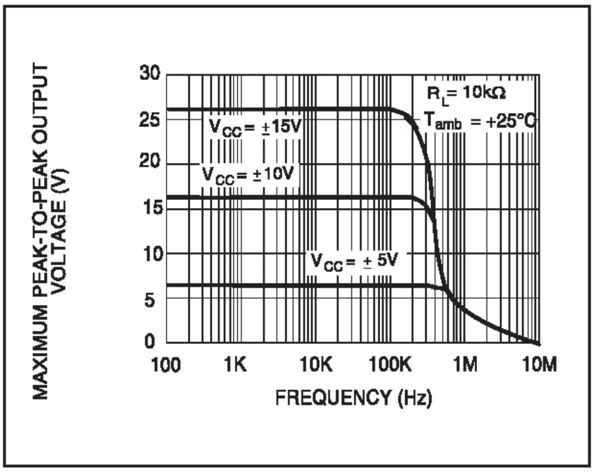
Symbol	Parameter	TL081I,M,AC,AI,AM, BC,BI,BM			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
THD	Total Harmonic Distortion (T_{amb} = +25°C), f= 1kHz, R_L = 2kΩ,C_L = 100pF, A_v = 20dB, V_o = 2V_{pp}		0.01			0.01		%
e_n	Equivalent Input Noise Voltage R_S = 100Ω, f = 1KHz		15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase Margin		45			45		degrees

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

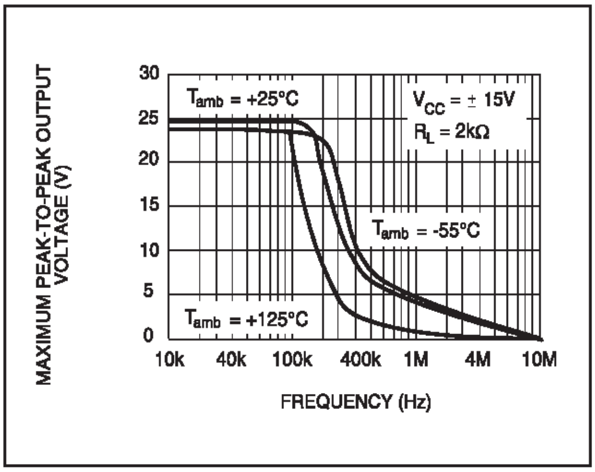
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



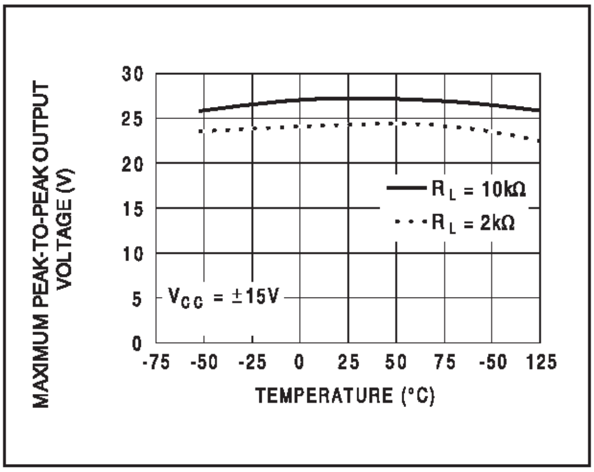
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



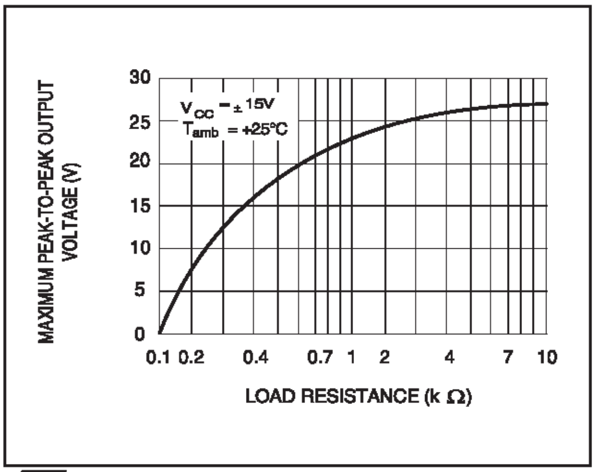
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



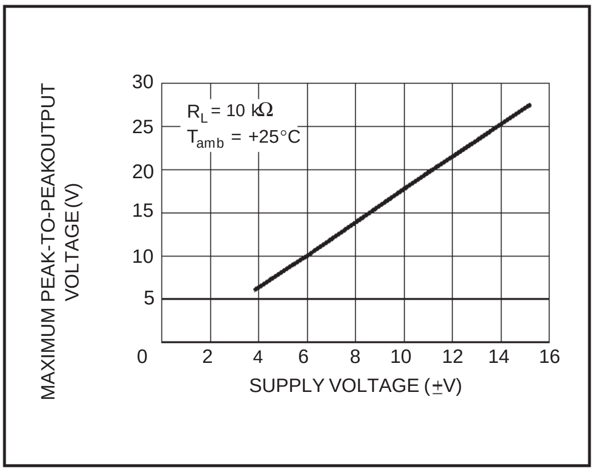
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREE AIR TEMP.



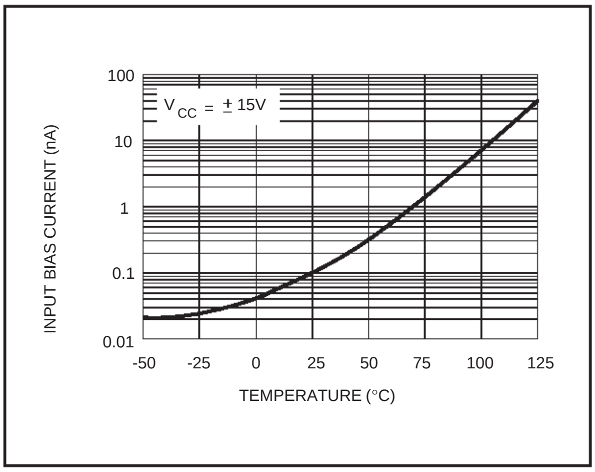
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus LOAD RESISTANCE



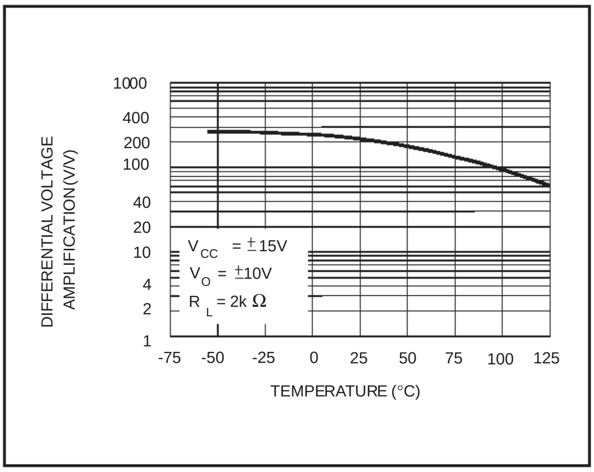
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus SUPPLY VOLTAGE



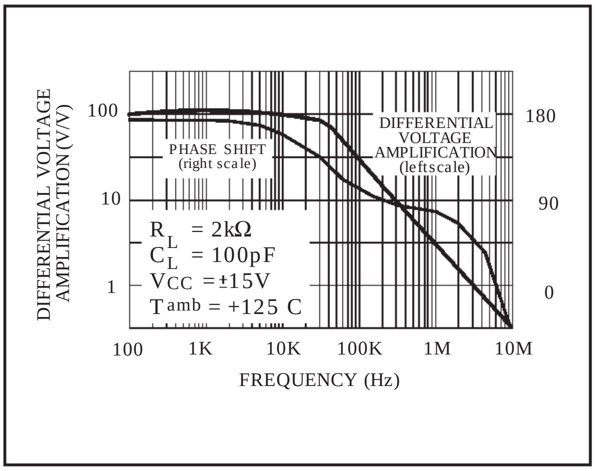
INPUT BIAS CURRENT versus FREE AIR TEMPERATURE



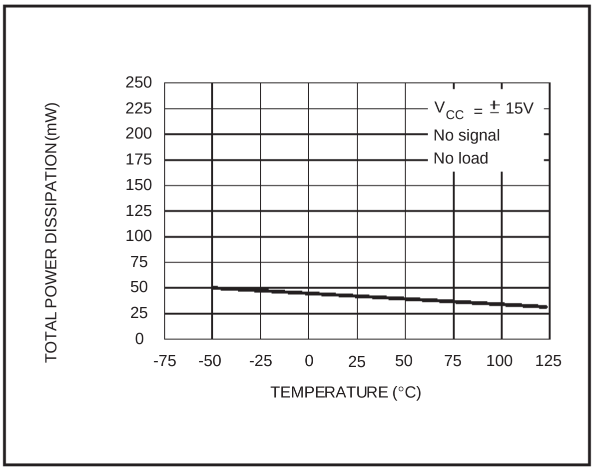
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION versus FREE AIR TEMP.



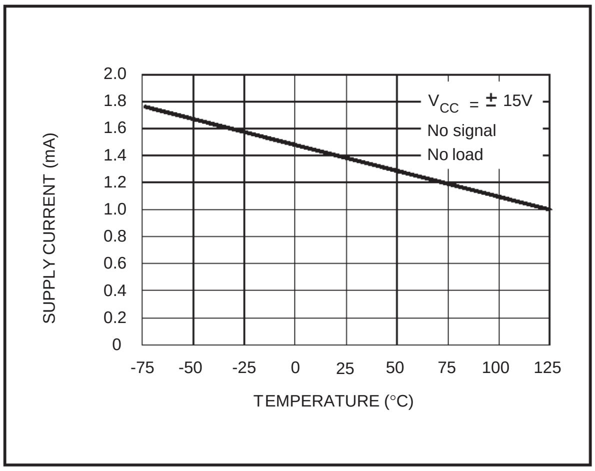
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT versus FREQUENCY



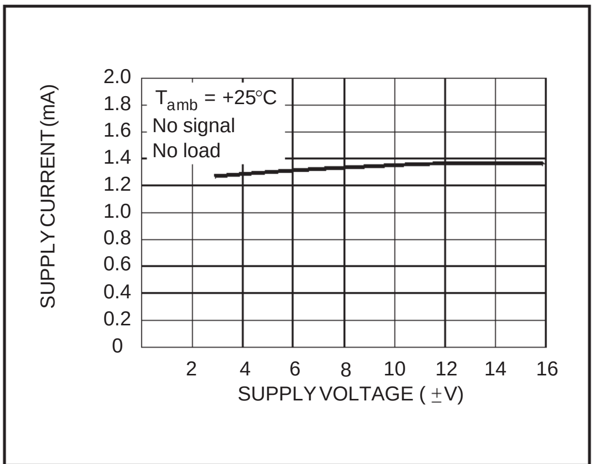
TOTAL POWER DISSIPATION versus FREE AIR TEMPERATURE



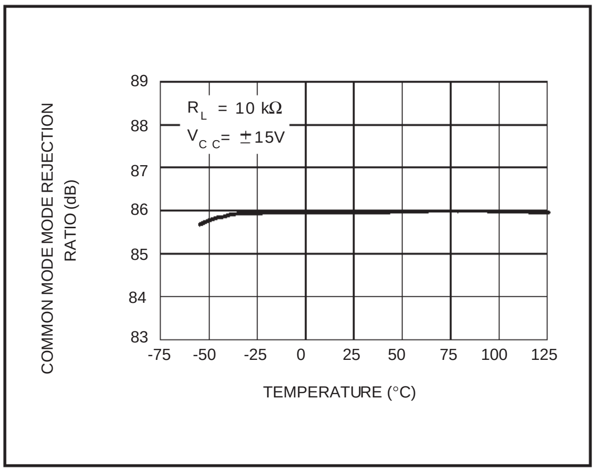
SUPPLY CURRENT PER AMPLIFIER versus FREE AIR TEMPERATURE



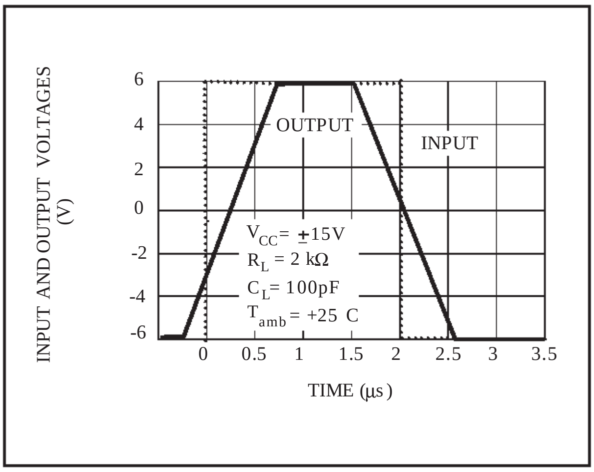
SUPPLY CURRENT PER AMPLIFIER versus SUPPLY VOLTAGE



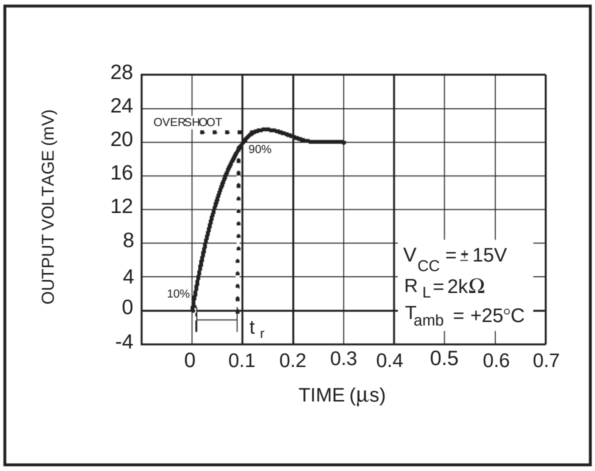
COMMON MODE REJECTION RATIO versus FREE AIR TEMPERATURE



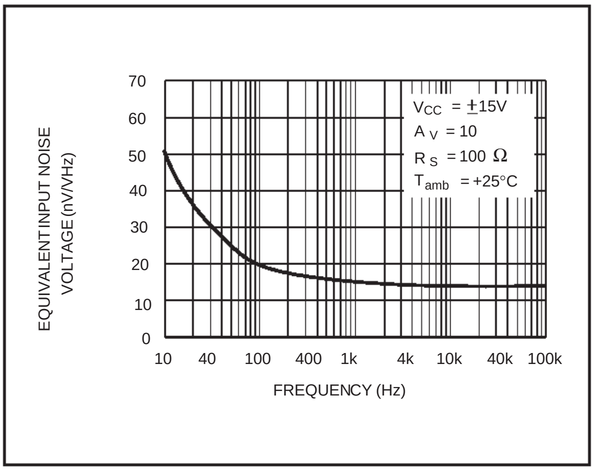
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



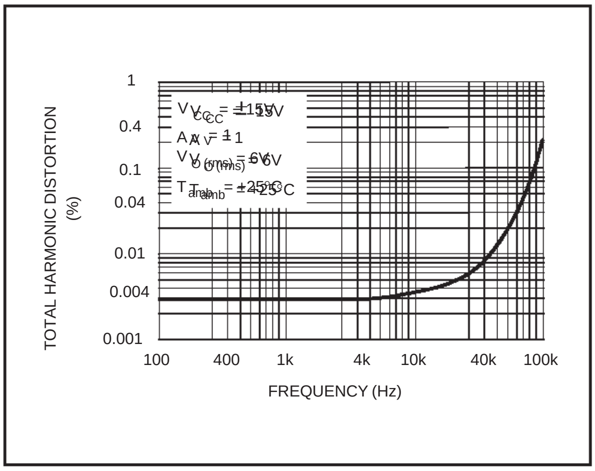
OUTPUT VOLTAGE versus ELAPSED TIME



EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY



TOTAL HARMONIC DISTORTION versus FREQUENCY



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

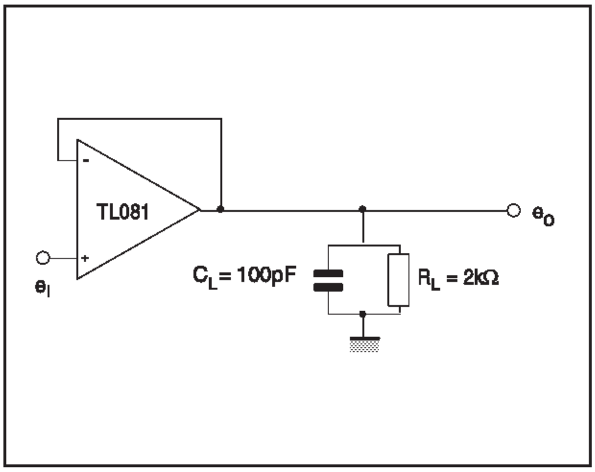
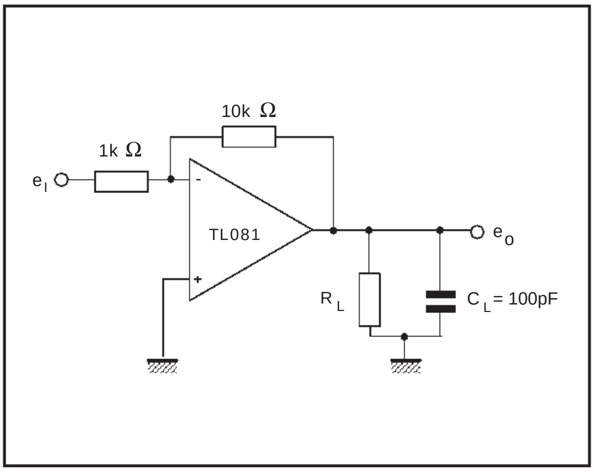
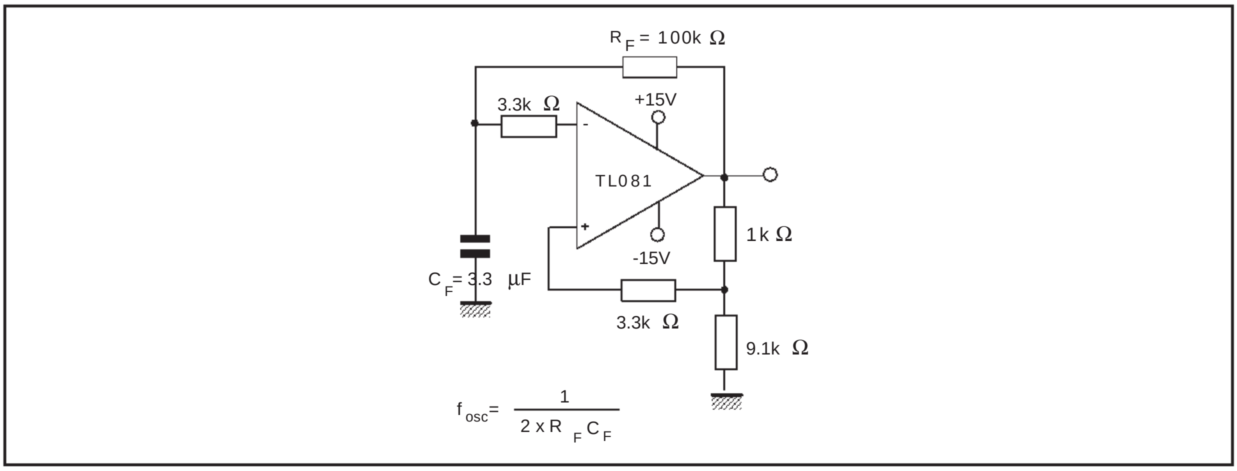


Figure 2 : Gain-of-10 Inverting Amplifier

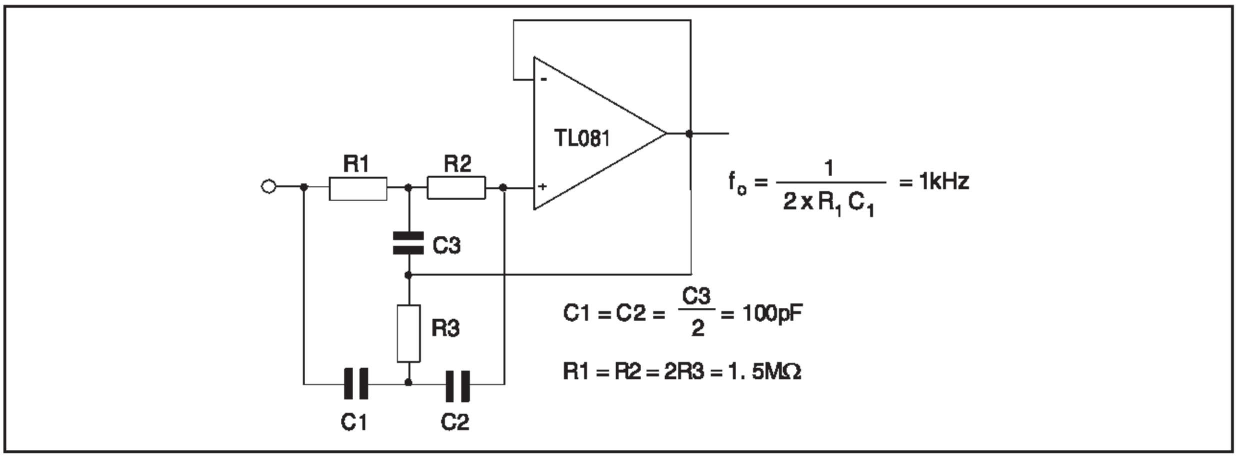


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR

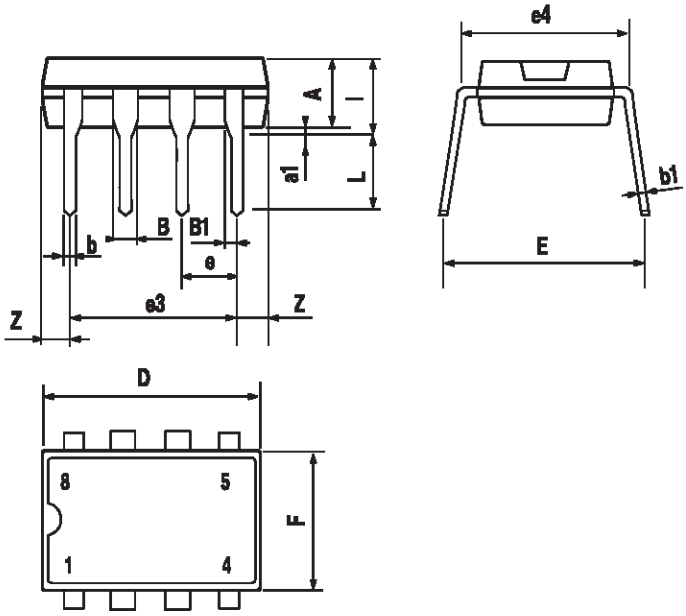


HIGH Q NOTCH FILTER



PACKAGE MECHANICAL DATA

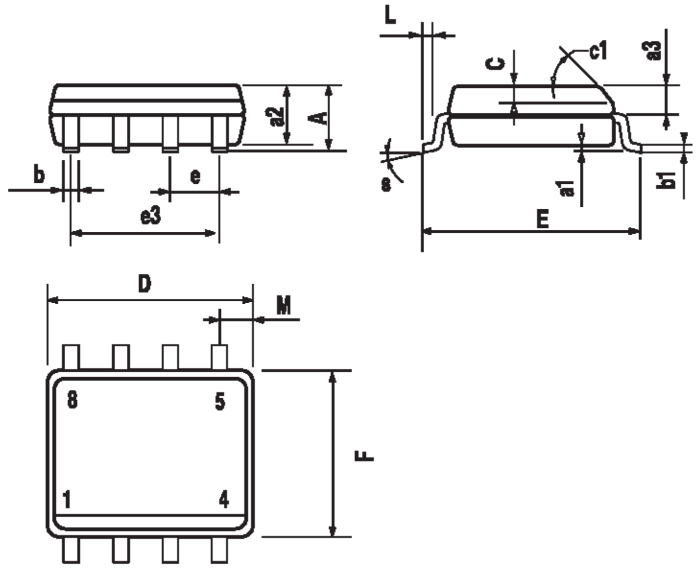
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT08

Quad 2-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} −1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

Quad 2-input AND gate 74HC/HCT08

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

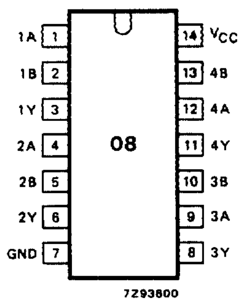


Fig.1 Pin configuration.

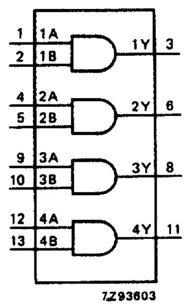


Fig.2 Logic symbol.

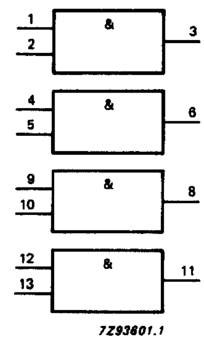


Fig.3 IEC logic symbol.

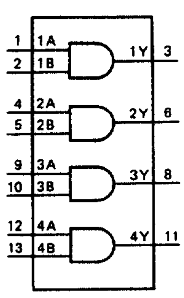


Fig.4 Functional diagram.

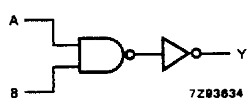


Fig.5 HC logic diagram (one gate).

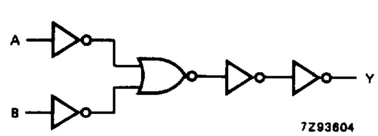


Fig.6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

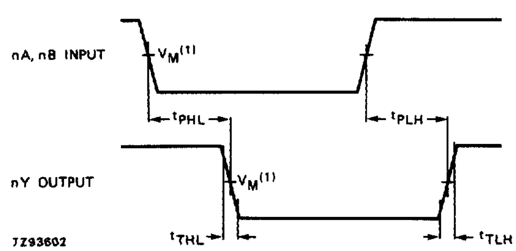
INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40106B gates
Hex inverting Schmitt trigger

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H).

This device may be used for enhanced noise immunity or to “square up” slowly changing waveforms.

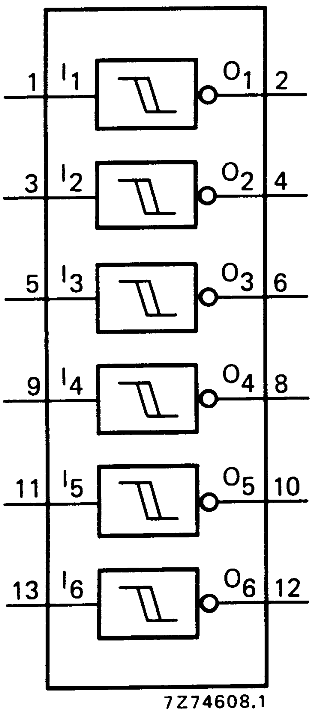


Fig.1 Functional diagram.

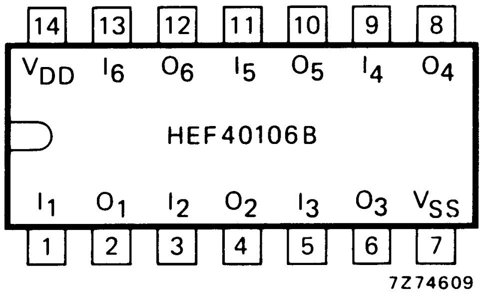


Fig.2 Pinning diagram.

HEF40106BP(N):	14-lead DIL; plastic (SOT27-1)
HEF40106BD(F):	14-lead DIL; ceramic (cerdip) (SOT73)
HEF40106BT(D):	14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

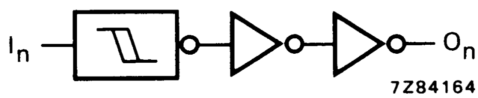


Fig.3 Logic diagram (one inverter).

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Hysteresis	5		0,5	0,8		V
voltage	10	V_H	0,7	1,3		V
	15		0,9	1,8		V
Switching levels	5		2	3,0	3,5	V
positive-going	10	V_P	3,7	5,8	7	V
input voltage	15		4,9	8,3	11	V
negative-going	5		1,5	2,2	3	V
input voltage	10	V_N	3	4,5	6,3	V
	15		4	6,5	10,1	V

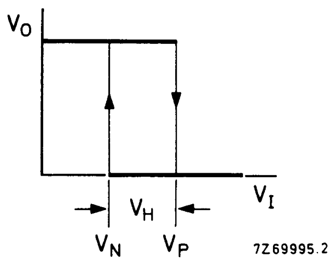


Fig.4 Transfer characteristic.

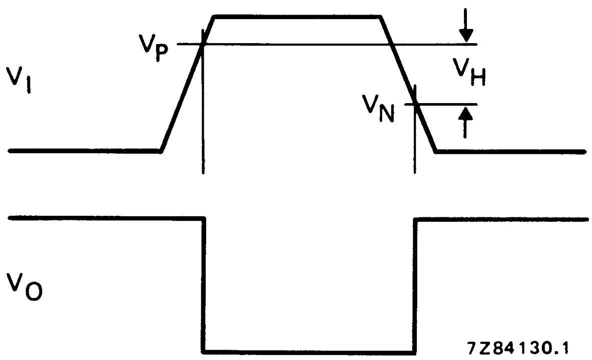


Fig.5 Waveforms showing definition of V_P, V_N and V_H, where V_N and V_P are between limits of 30% and 70%.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n$	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF)
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$2\,300\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$9\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$20\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

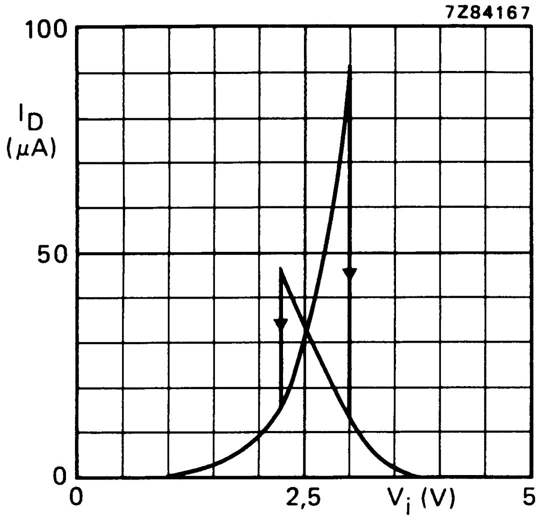


Fig.6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

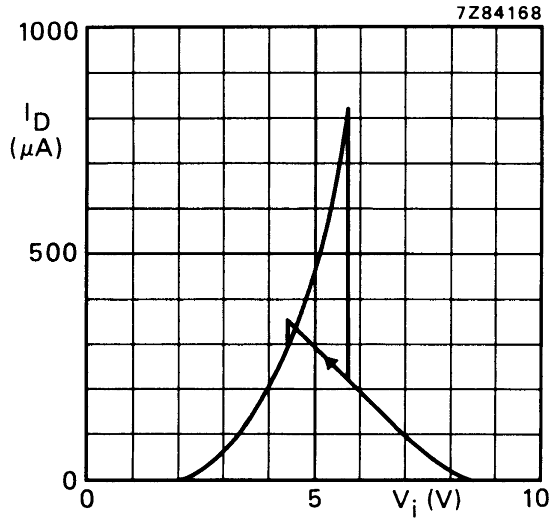


Fig.7 Typical drain current as a function of input voltage; V_{DD} =10 V; T_{amb} = 25 °C.

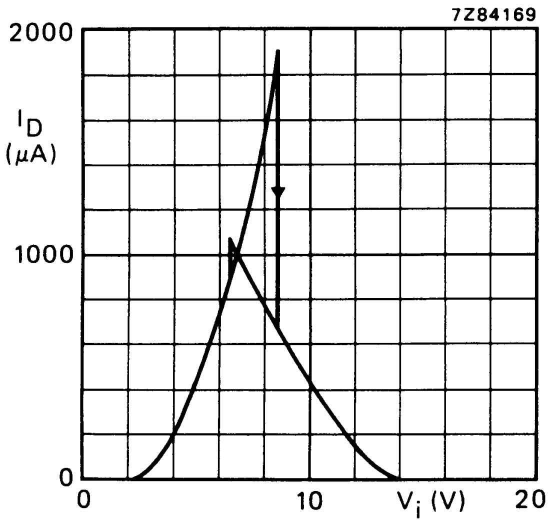


Fig.8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

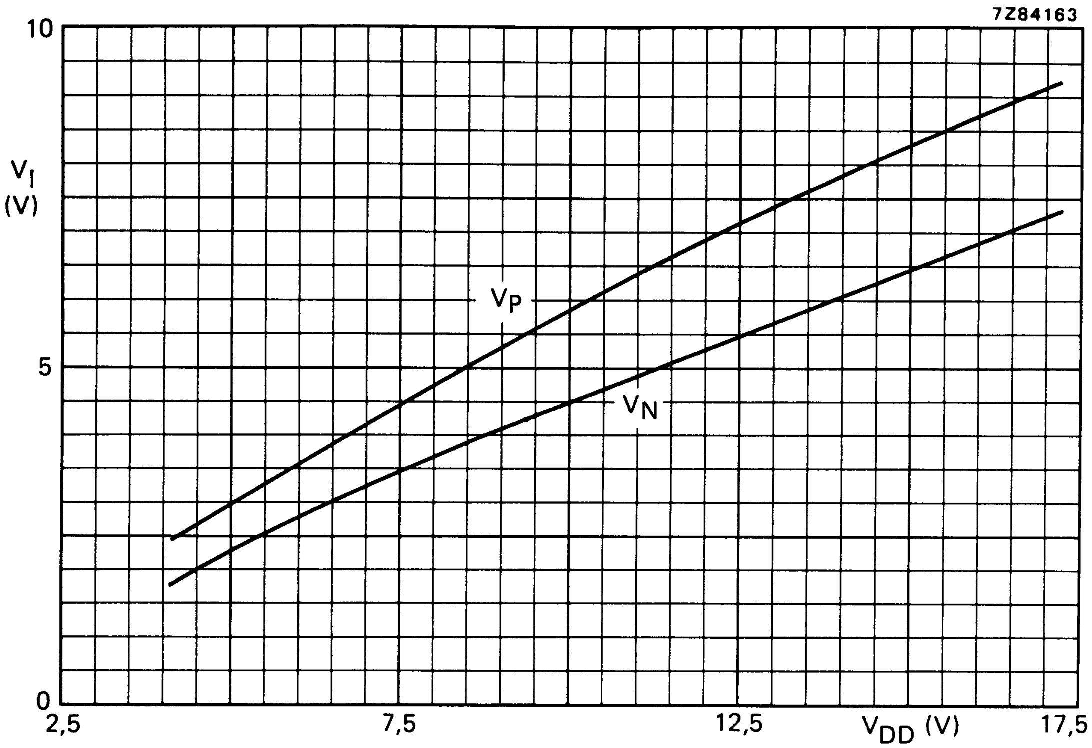


Fig.9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

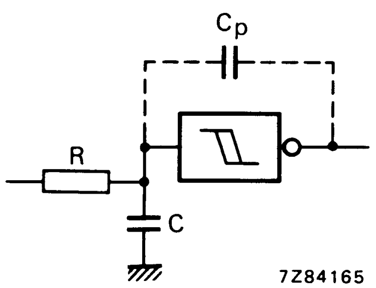


Fig.10 Schmitt trigger driven via a high impedance (R > 1 kΩ).

If a Schmitt trigger is driven via a high impedance (R > 1 kΩ) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

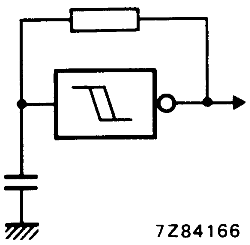
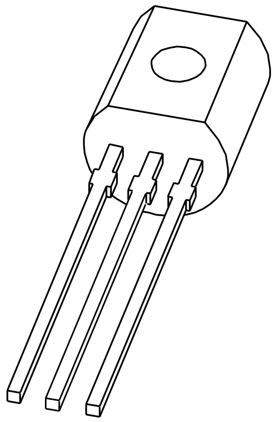


Fig.11 The HEF40106B used as an astable multivibrator.

DISCRETE SEMICONDUCTORS

DATA SHEET



BC546; BC547
NPN general purpose transistors

Product specification
Supersedes data of 1997 Mar 04

1999 Apr 15

NPN general purpose transistors | BC546; BC547

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

NPN transistor in a TO-92; SOT54 plastic package.
PNP complements: BC556 and BC557.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

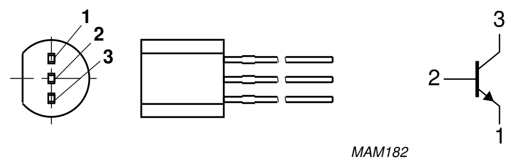


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC546		–	80	V
	BC547		–	50	V
V_{CEO}	collector-emitter voltage	open base			
	BC546		–	65	V
	BC547		–	45	V
V_{EBO}	emitter-base voltage	open collector			
	BC546		–	6	V
	BC547		–	6	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

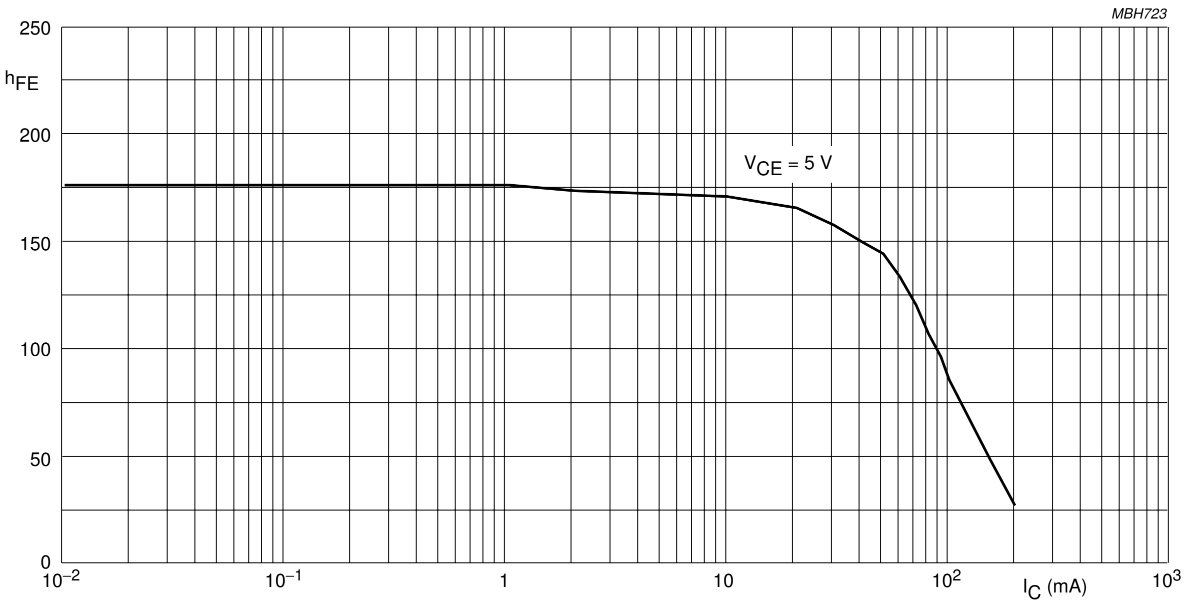
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 30$ V	–	–	15	nA
		$I_E = 0$; $V_{CB} = 30$ V; $T_j = 150$ °C	–	–	5	μA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 5$ V	–	–	100	nA
h_{FE}	DC current gain	$I_C = 10$ μA; $V_{CE} = 5$ V; see Figs 2, 3 and 4				
	BC546A		–	90	–	
	BC546B; BC547B		–	150	–	
	BC547C		–	270	–	
	DC current gain	$I_C = 2$ mA; $V_{CE} = 5$ V; see Figs 2, 3 and 4				
	BC546A		110	180	220	
	BC546B; BC547B		200	290	450	
	BC547C		420	520	800	
	BC547		110	–	800	
	BC546		110	–	450	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10$ mA; $I_B = 0.5$ mA	–	90	250	mV
		$I_C = 100$ mA; $I_B = 5$ mA	–	200	600	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10$ mA; $I_B = 0.5$ mA; note 1	–	700	–	mV
		$I_C = 100$ mA; $I_B = 5$ mA; note 1	–	900	–	mV
V_{BE}	base-emitter voltage	$I_C = 2$ mA; $V_{CE} = 5$ V; note 2	580	660	700	mV
		$I_C = 10$ mA; $V_{CE} = 5$ V	–	–	770	mV
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = 10$ V; f = 1 MHz	–	1.5	–	pF
C_e	emitter capacitance	$I_C = i_c = 0$; $V_{EB} = 0.5$ V; f = 1 MHz	–	11	–	pF
f_T	transition frequency	$I_C = 10$mA; $V_{CE} = 5$ V; f = 100 MHz	100	–	–	MHz
F	noise figure	$I_C = 200$ μA; $V_{CE} = 5$ V; $R_S = 2$ kΩ; f = 1 kHz; B = 200 Hz	–	2	10	dB

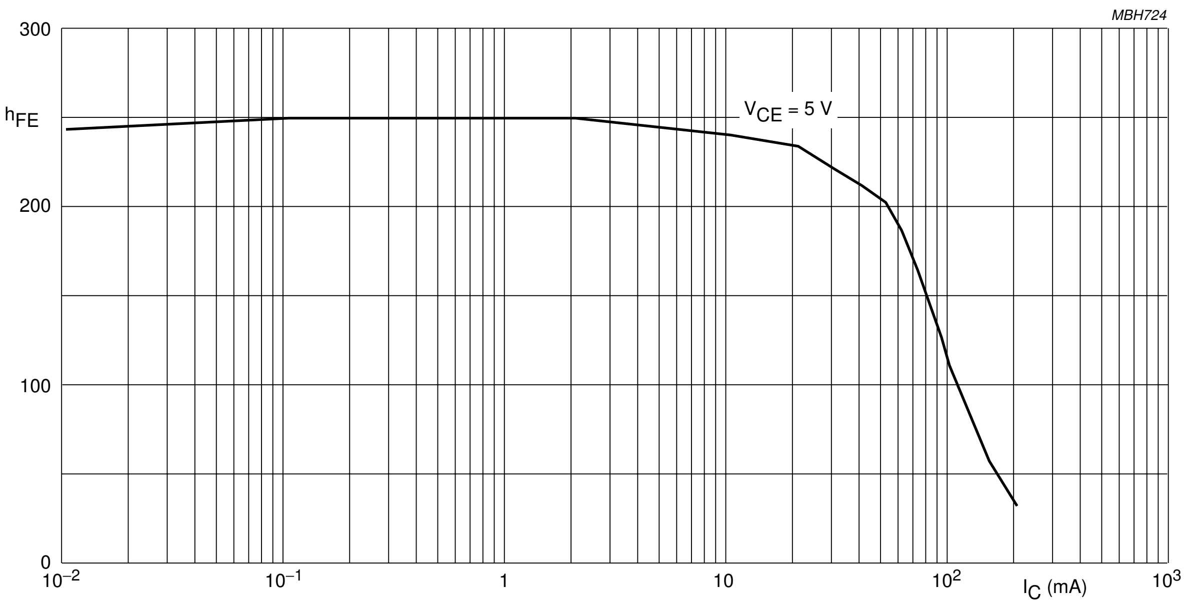
Notes

1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
2. V_{BE} decreases by about 2 mV/K with increasing temperature.



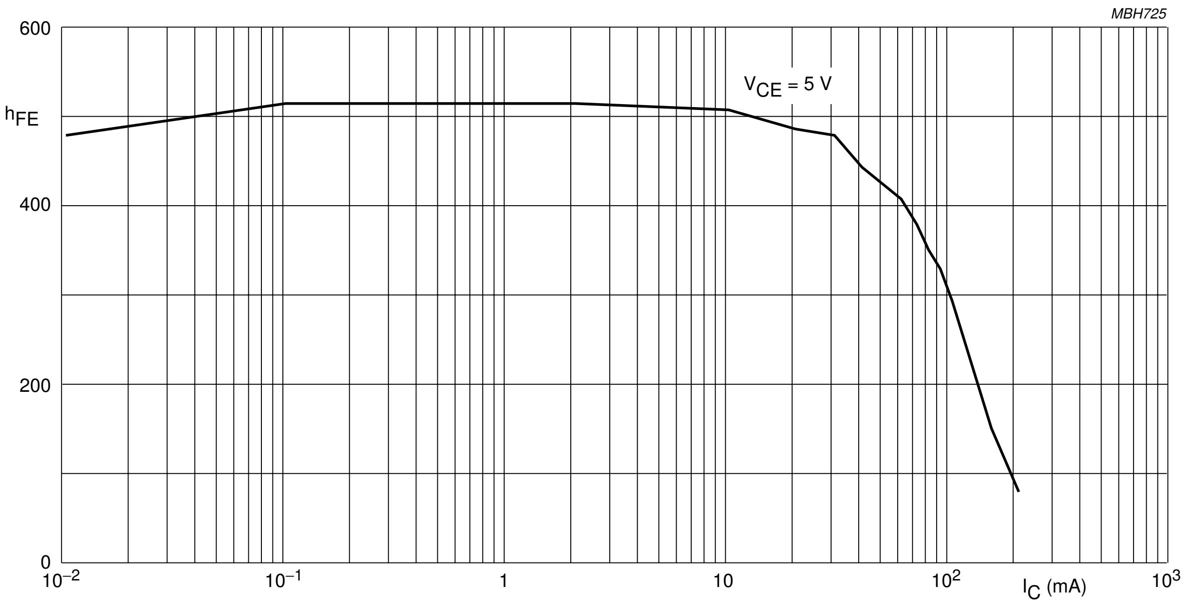
BC546A.

Fig.2 DC current gain; typical values.



BC546B; BC547B.

Fig.3 DC current gain; typical values.

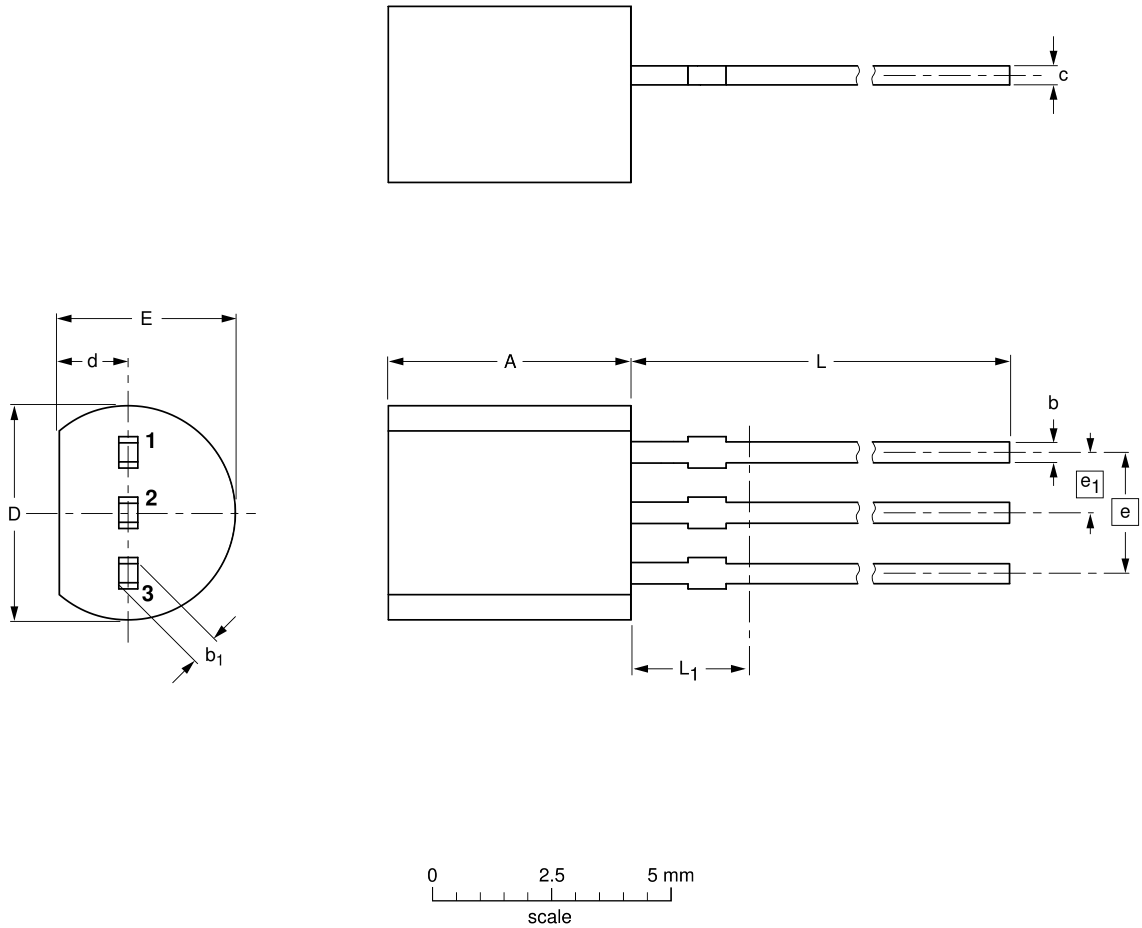


BC547C.

Fig.4 DC current gain; typical values.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**

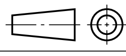


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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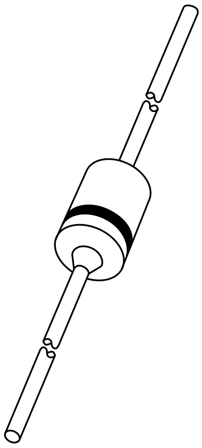
DATA SHEET



1N4001ID to 1N4007ID
Rectifiers

Product specification
Supersedes data of April 1992

1996 Jun 10

Philips
Semiconductors

PHILIPS

Rectifiers 1N4001ID to 1N4007ID

FEATURES

- Glass passivated
- High maximum operating temperature
- Low leakage current
- Excellent stability
- Available in ammo-pack.

DESCRIPTION

Cavity free cylindrical glass package through Implotec™(1) technology.

This package is hermetically sealed and fatigue free as coefficients of expansion of all used parts are matched.

(1) Implotec is a trademark of Philips.

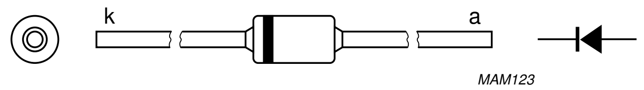


Fig.1 Simplified outline (SOD81) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage				
	1N4001ID		–	50	V
	1N4002ID		–	100	V
	1N4003ID		–	200	V
	1N4004ID		–	400	V
	1N4005ID		–	600	V
	1N4006ID		–	800	V
	1N4007ID		–	1000	V
V_R	continuous reverse voltage				
	1N4001ID		–	50	V
	1N4002ID		–	100	V
	1N4003ID		–	200	V
	1N4004ID		–	400	V
	1N4005ID		–	600	V
	1N4006ID		–	800	V
	1N4007ID		–	1000	V
$I_{F(AV)}$	average forward current	averaged over any 20 ms period; T_{amb} = 75 °C; see Fig.2	–	1.00	A
		averaged over any 20 ms period; T_{amb} = 100 °C; see Fig.2	–	0.75	A
I_{FRM}	repetitive peak forward current		–	10	A
I_{FSM}	non-repetitive peak forward current	half sinewave; 60 Hz	–	20	A
T_{stg}	storage temperature		–65	+175	°C
T_j	junction temperature		–65	+175	°C

ELECTRICAL CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 1 A; see see Fig.3	1.1	V
$V_{F(AV)}$	full-cycle average forward voltage	$I_{F(AV)}$ = 1 A	0.8	V
I_R	reverse current	$V_R = V_{Rmax}$	10	μA
		$V_R = V_{Rmax}$; T_{amb} = 100 °C	50	μA
$I_{R(AV)}$	full-cycle average reverse current	$V_R = V_{RRMmax}$; T_{amb} = 75 °C	30	μA

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length = 10 mm	60	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	120	K/W

Note

1. Device mounted on epoxy-glass printed-circuit board, 1.5 mm thick; thickness of copper ≥40 μm, see Fig.4. For more information please refer to the *"General Part of associated Handbook"*.

GRAPHICAL DATA

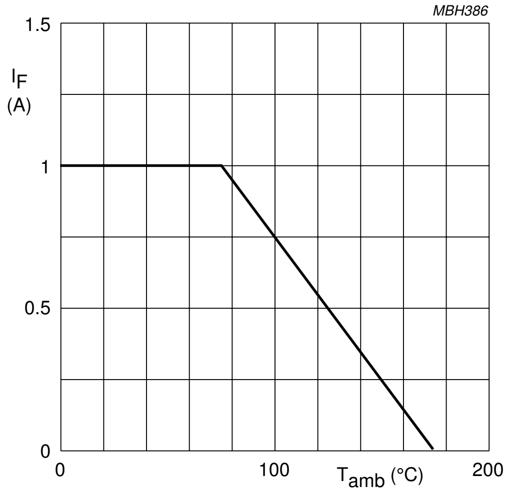
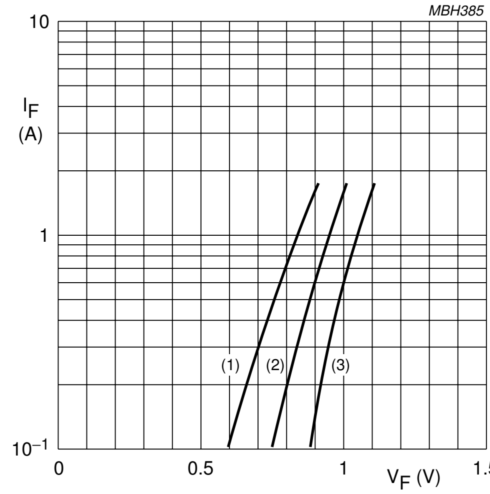
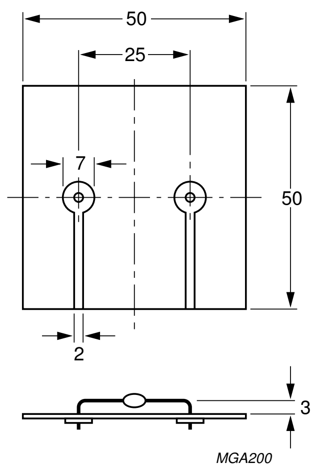


Fig.2 Maximum forward current as a function of ambient temperature.



(1) T_{amb} = 100 °C.
(2) T_{amb} = 20 °C.
(3) T_{amb} = −50 °C.

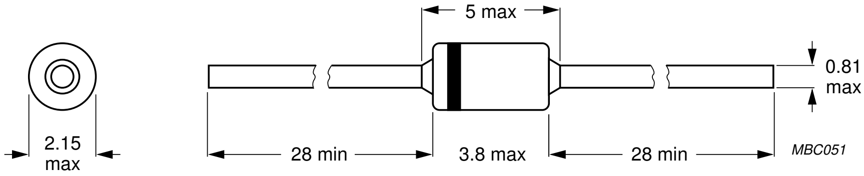
Fig.3 Forward current as a function of forward voltage; typical values.



Dimensions in mm.

Fig.4 Device mounted on a printed-circuit board.

PACKAGE OUTLINE



Dimensions in mm.

Fig.5 SOD81.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

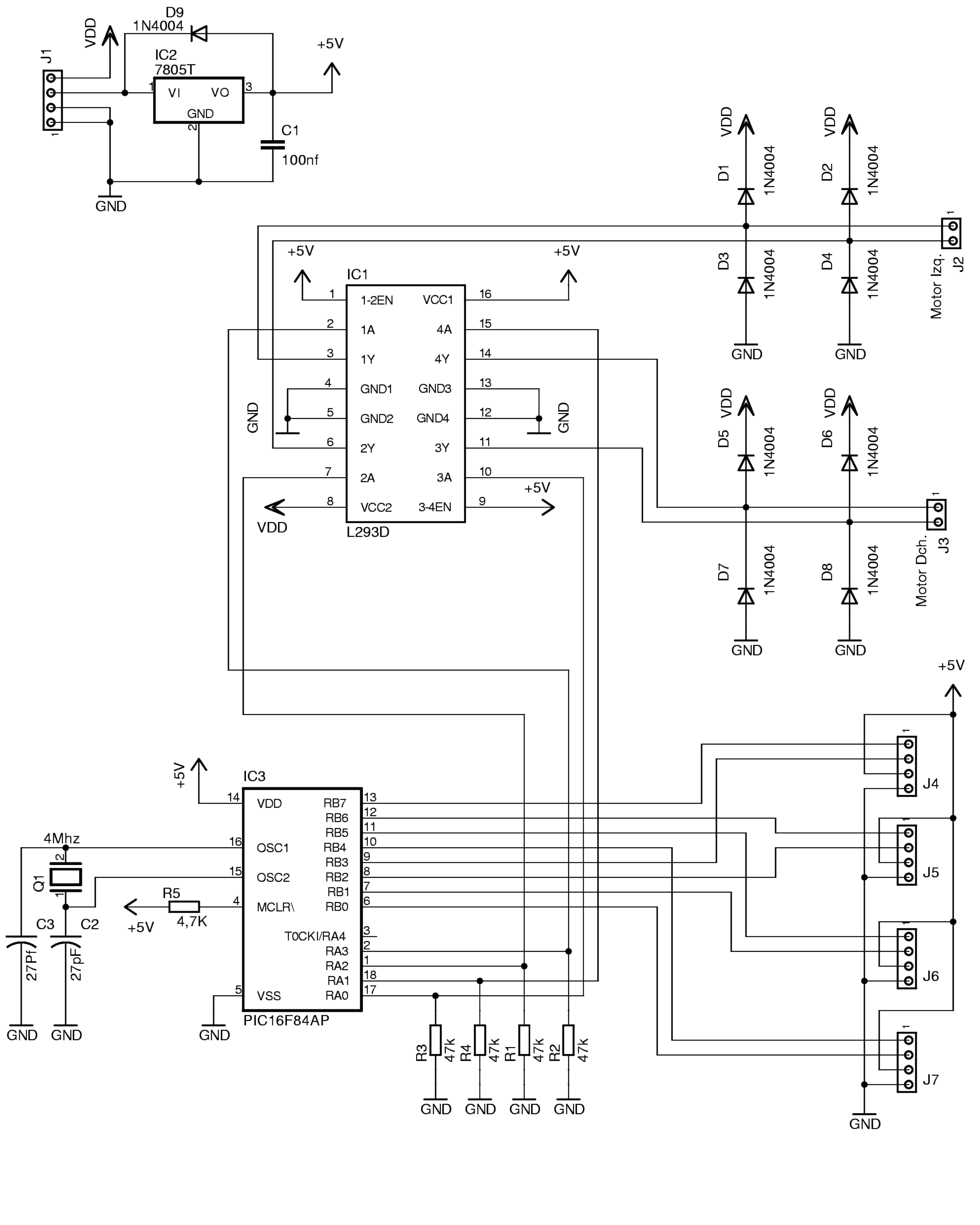
LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Parte II

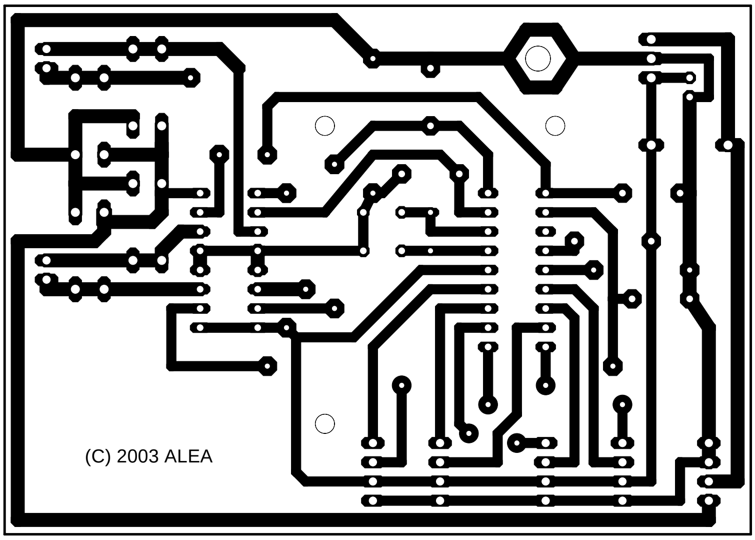
Planos

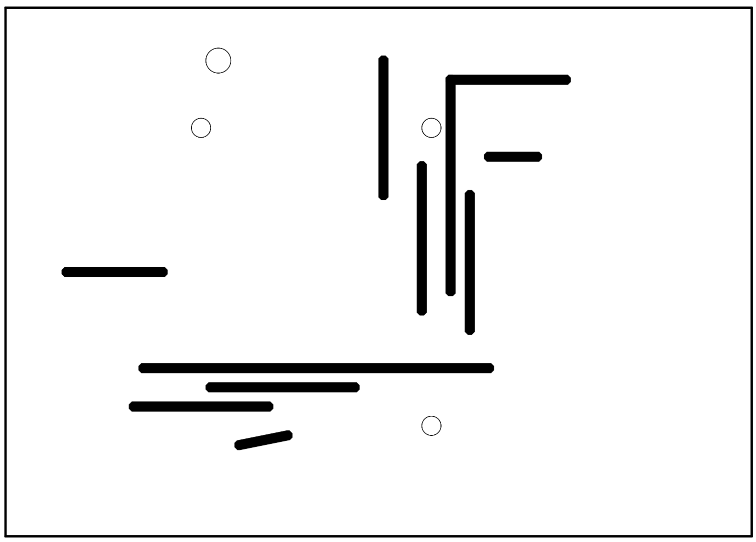
Tabla de Contenidos

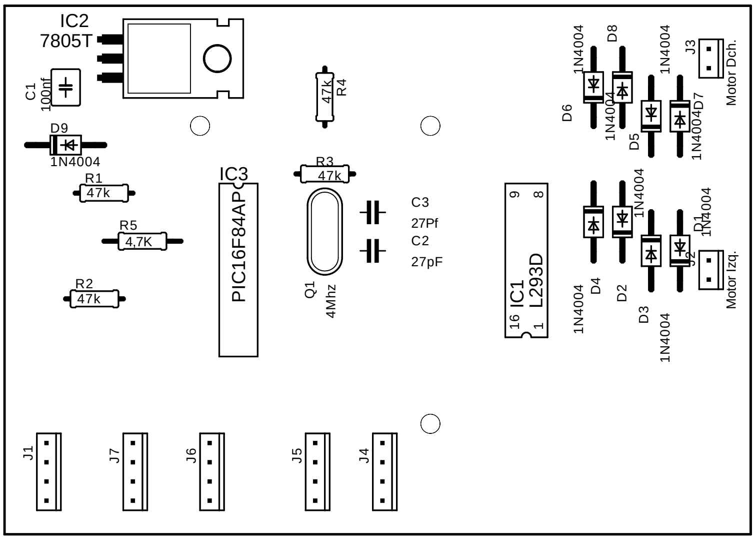


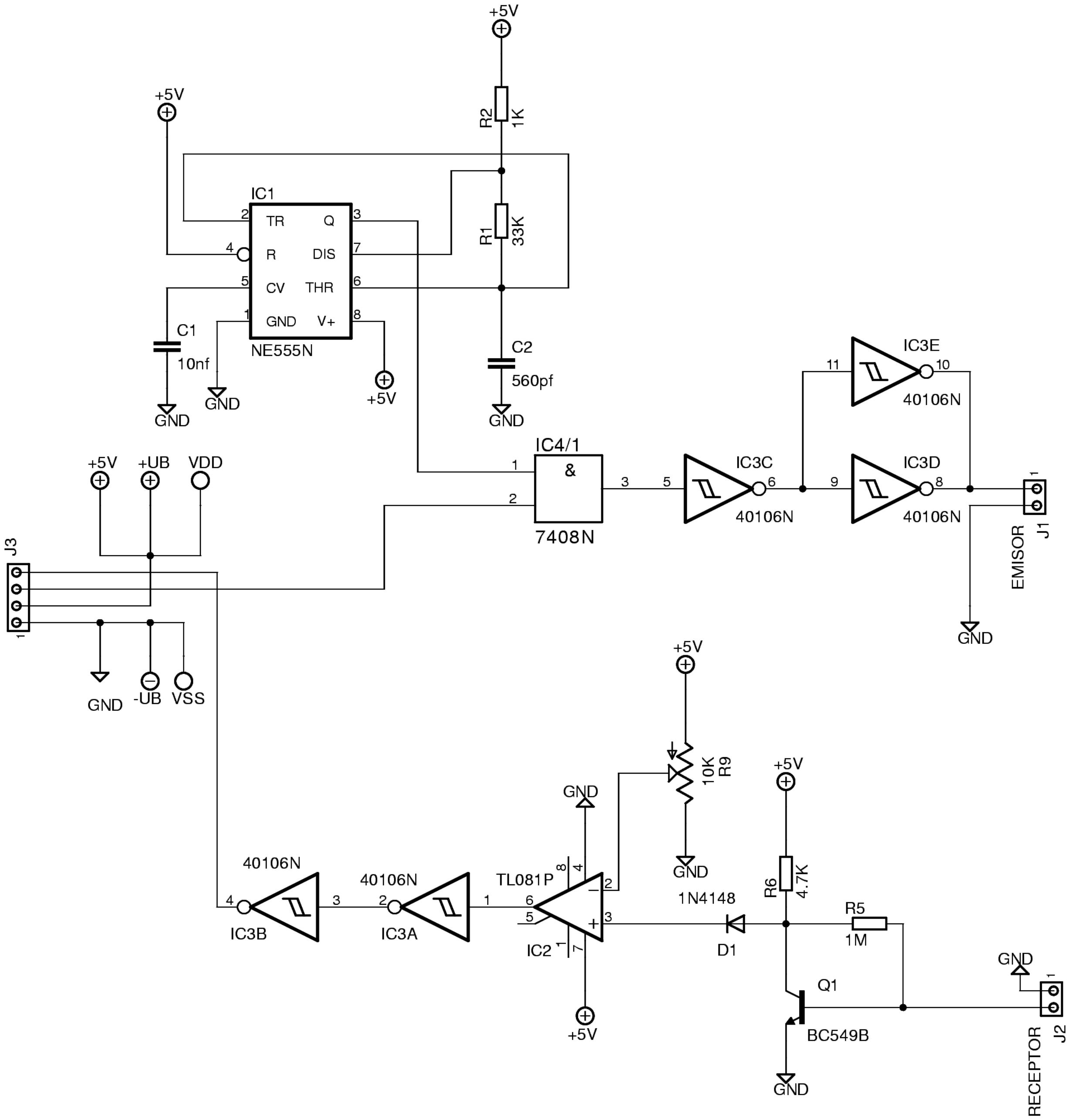
	Fecha	Nombre	Firma	ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON
Disenado	6/6/2003	Alvaro Alea Fernandez		
Dibujado	10/6/2003	Alvaro Alea Fernandez		
Comprobado				

Escala	Robot Controlado por Ultrasonidos	Revision: 1
1:1	C. Principal - Esquema	Hoja 1 de 12


(C) 2003 ALEA

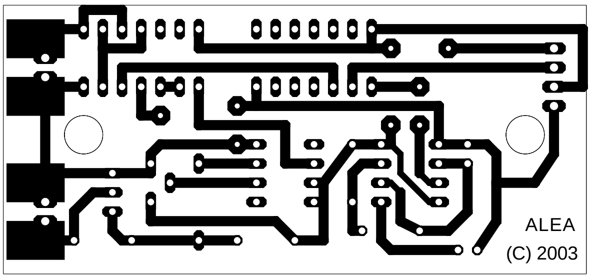


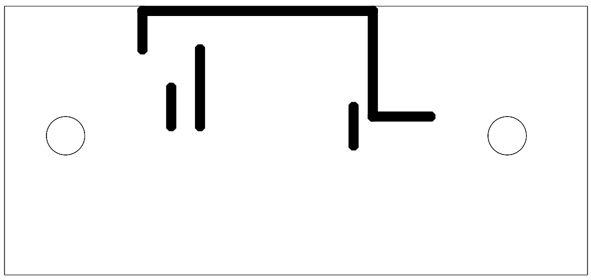

IC2
7805T
C1
100nf
R4
47k
D9
1N4004
R1
47k
IC3
PIC16F84AP
R3
47k
R5
4,7K
R2
47k
Q1
4Mhz
C3
27Pf
C2
27pF
IC1
L293D
D6
D8
D5
D7
D4
D2
D3
D1
1N4004
J3
Motor Dch.
J2
Motor Izq.
J1
J7
J6
J5
J4

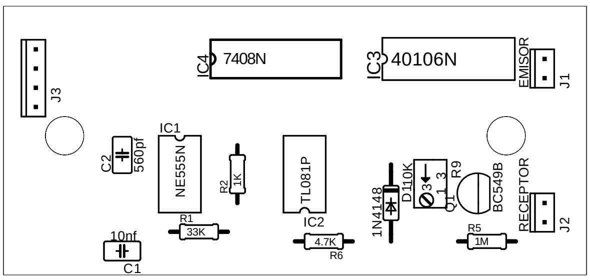


	Fecha	Nombre	Firma	ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON
Disenado		Alvaro Alea Fernandez		
Dibujado		Alvaro Alea Fernandez		
Comprobado				

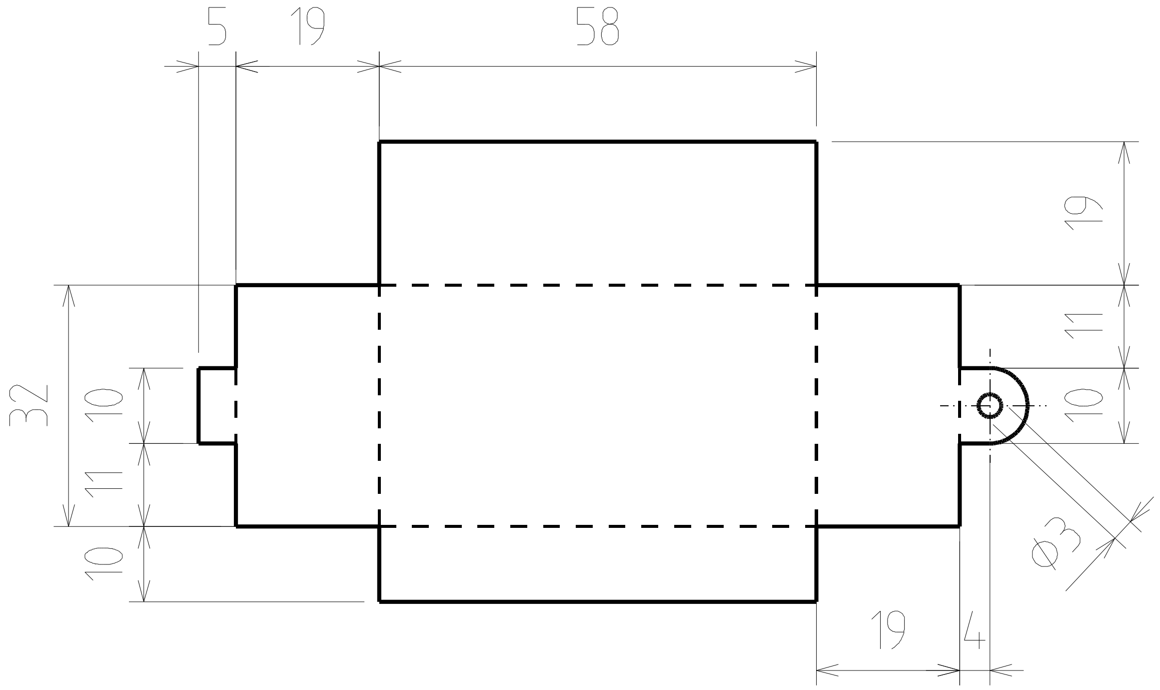
Escala	Robot Controlado por Ultrasonidos	Revision: 2
1:1	C. Sensores -Esquema	Hoja 5 de 12

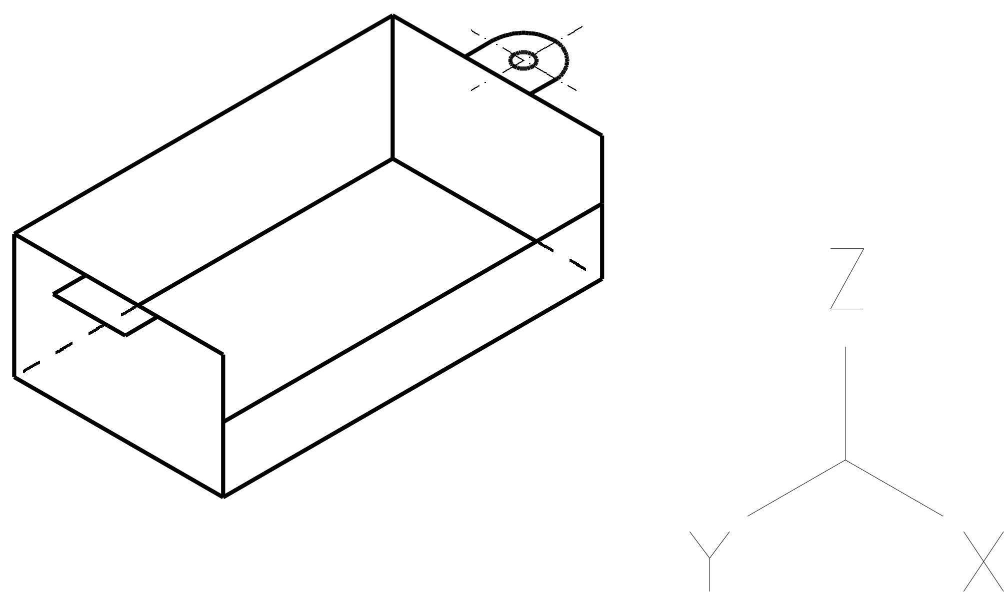

ALEA
(C) 2003





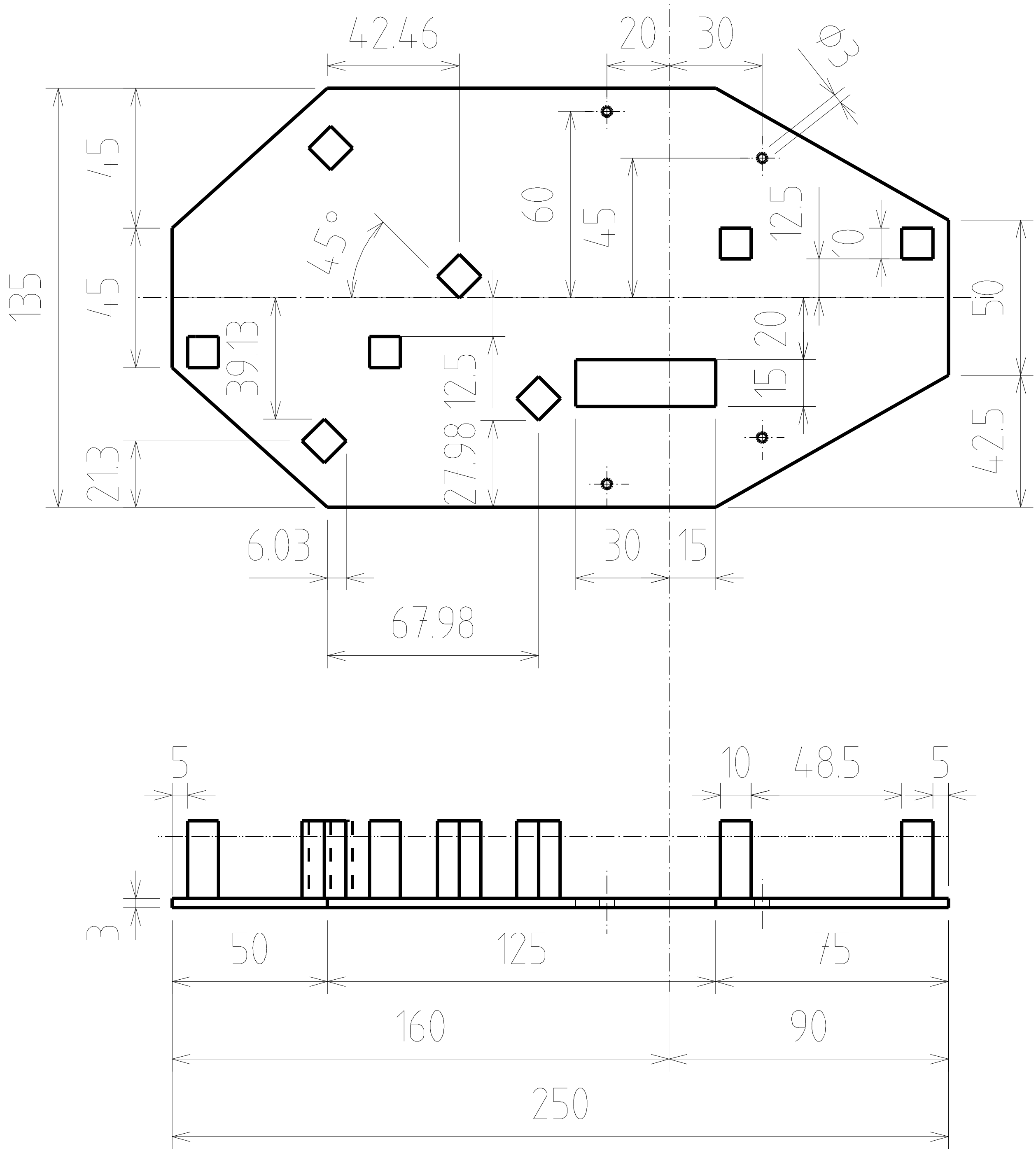
J3
7408N
IC4
40106N
IC3
EMISOR
J1
C2
560pf
IC1
NE555N
R2
1K
TL081P
IC2
1N4148
D1
10K
R9
BC549B
Q1
RECEPTOR
J2
R1
33K
4.7K
R6
R5
1M
10nf
C1





	Fecha	Nombre	Firma	ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON
Disenado	6/6/2003	Alvaro Alea Fernandez		
Dibujado	10/6/2003	Alvaro Alea Fernandez		
Comprobado				

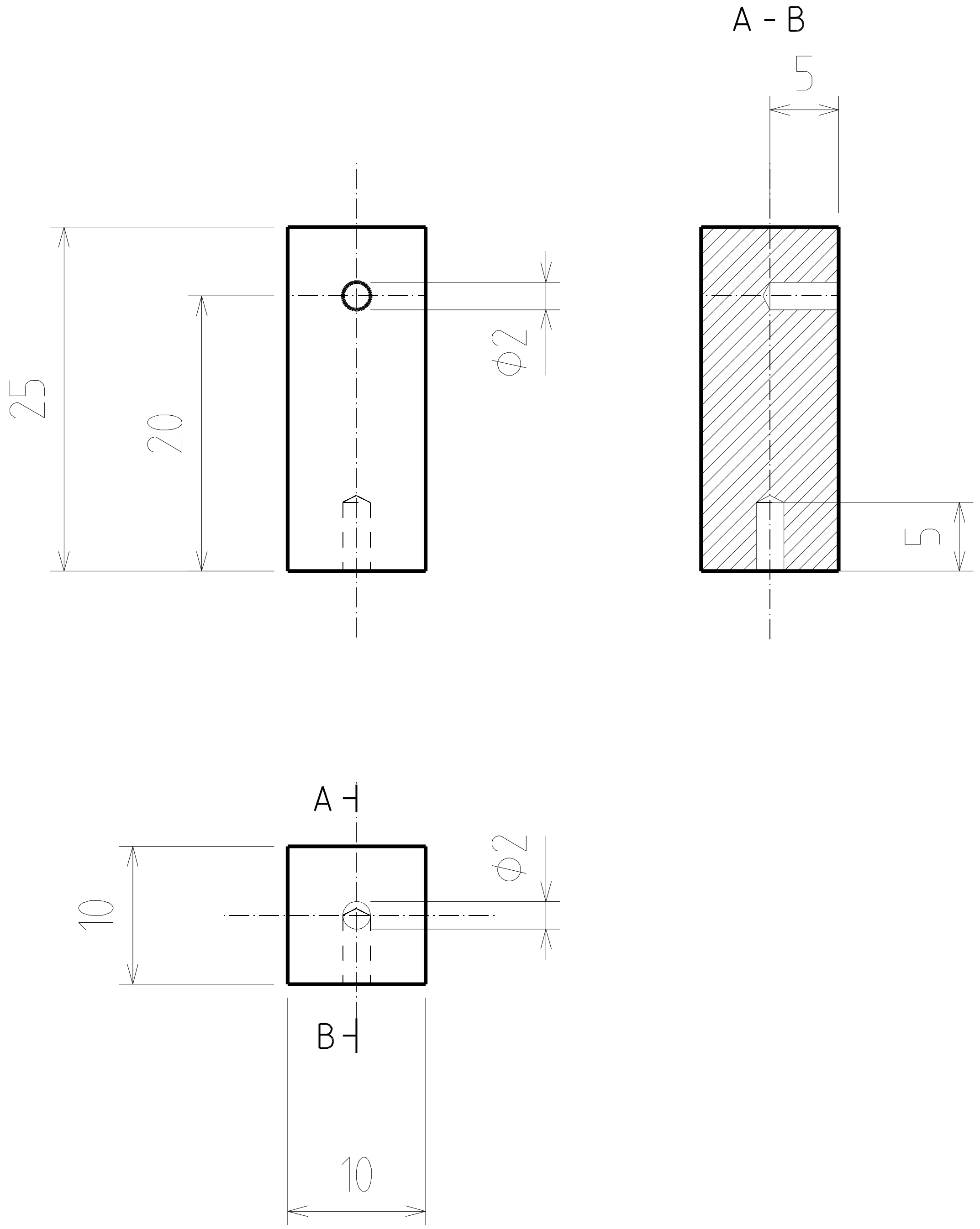
Escala		
1:1	Robot Controlado por Ultrasonidos	Revision: 1
	Soporte de Sensores - Portapilas	Hoja 9 de 12



	Fecha	Nombre	Firma
Disenado	6/6/2003	Alvaro Alea Fernandez	
Dibujado	10/6/2003	Alvaro Alea Fernandez	
Comprobado			

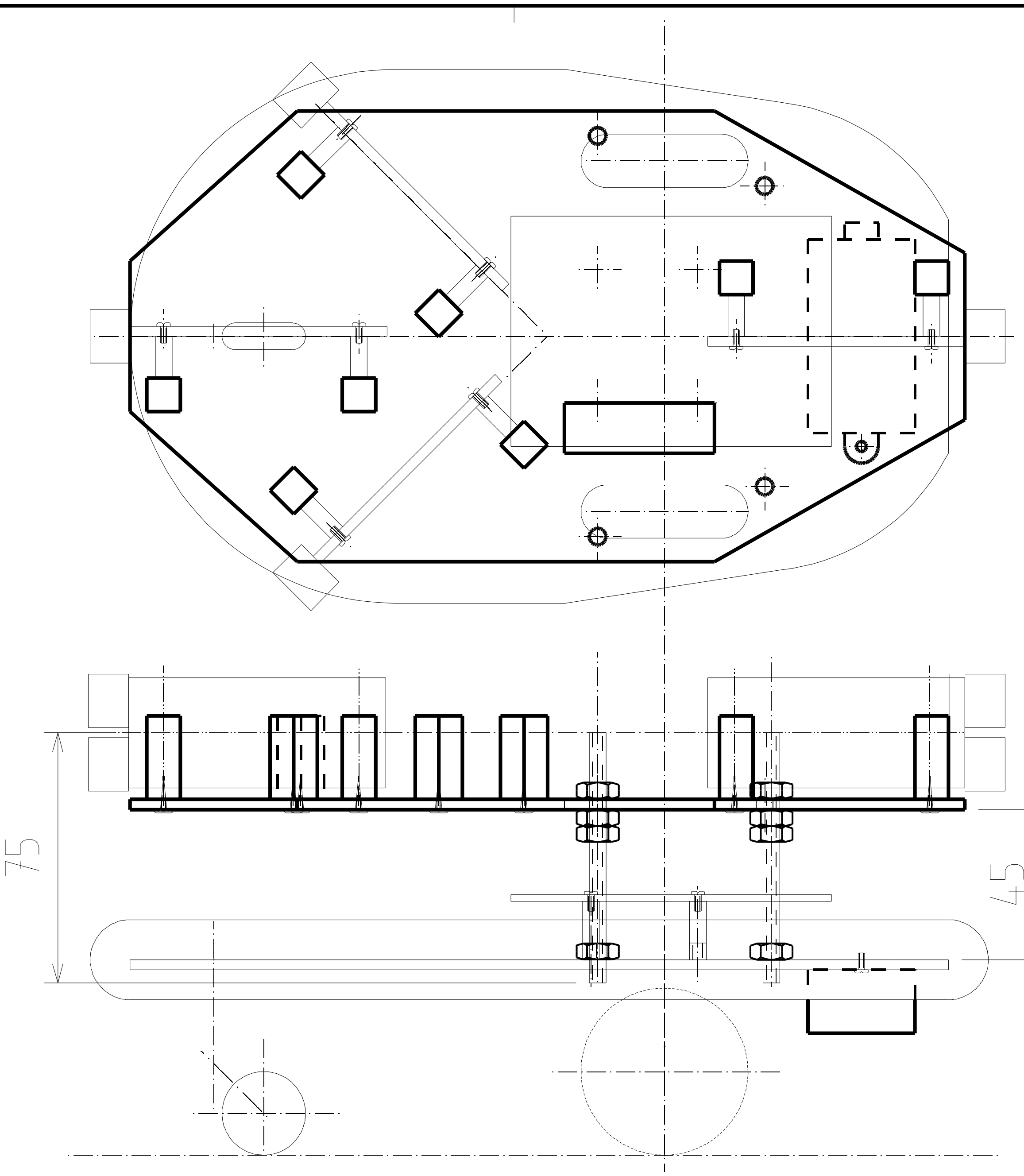
ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON

Escala	Título	
1:2	Robot Controlado por Ultrasonidos	Revision: 1
	Soporte de Sensores - Dimensiones	Hoja 10 de 12



	Fecha	Nombre	Firma	ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON
Disenado	10/8/2003	Alvaro Alea Fernandez		
Dibujado	15/8/2003	Alvaro Alea Fernandez		
Comprobado				

Escala	Robot Controlado por Ultrasonidos	Rev: 1
2:1	Soporte de Sensores - Taco	Hoja 11 de 12



Referencia	Cantidad	Denominacion
	1	Circuito Impreso Placa Central
	11	Separadores de Circuito Impreso M3 1/2''
	8	Tirafondo 10mm
	8	Taco
	1	Soporte Sensores
	1	Portapilas
	1	Base Robot
	4	Varilla Roscada M3 x 75mm
	16	Tuerca M3
	12	Tornillo M3 x 10mm

	Fecha	Nombre	Firma
Disenado	6/6/2003	Alvaro Alea Fernandez	
Dibujado	10/6/2003	Alvaro Alea Fernandez	
Comprobado			

ESCUELA UNIVERSITARIA DE INGENIERIA TECNICA INDUSTRIAL DE GIJON

Escala 1:2

Robot Controlado por Ultrasonidos

Soporte de Sensores - Disposicion

Revision: 1

Hoja 12 de 12

Parte III

Pliego de Condiciones

Tabla de Contenidos

Capítulo 13
Pliego de Condiciones

El presente pliego de condiciones define los requisitos que se han de seguir en la dirección, construcción y control del proyecto.

13.1. Condiciones Legales

El presente documento, y el resto de documentos que forman este proyecto, incluyendo planos y presupuesto, contemplan las condiciones que han de cumplir los materiales y su mano de obra, instrucciones para su ejecución y normas a seguir.

La consecución de todos los permisos y licencias que se estimen necesarias para la realización del citado proyecto corren a cargo de la empresa o sus representantes legales.

La empresa que decida fabricar este proyecto deberá correr con los gastos de homologación del producto y patentes que sean posibles realizar en el registro industrial.

La homologación y patentes figuraran bajo el nombre del proyectista y en ningún caso de la empresa que lo realice.

El programa software suministrado en el proyecto es propiedad intelectual del proyectista, según establecen las leyes de derechos de autor (copyright) y suministrado bajo licencia General Public License Versión 2 (GPL). La cesión de los derechos de autor bajo una licencia diferente deberá ser negociada con el proyectista de manera independiente a este proyecto.

13.2. Especificaciones de los Materiales

Todos los materiales empleados para la fabricación del microbot descrito en este proyecto deben ser los que se detallan en la lista de materiales, debiendo cumplir estos los valores y tolerancias que se especifiquen para cada componente.

El fabricante al cual se haga el pedido de materiales no es relevante siempre que cumpla lo anteriormente expuesto.

Para realizar cualquier cambio en alguno de los componentes que se detallan en la lista de materiales se consultara con el proyectista, este declina toda responsabilidad sobre el mal funcionamiento del producto sobre quien haya autorizado dicho cambio.

Antes de proceder al ensamblaje de los componentes en la placas de circuito impreso, cada componente debe ser comprobado para verificar que cumple la tolerancia y valores que nos asegure el fabricante del mismo, de no cumplirse los requisitos, estos deben ser remplazados por otros que si los cumplan, el proyectista no se hace cargo de problemas derivados de esta circunstancia.

13.3. Especificaciones de Construcción y Ejecución

Las placas de circuito impreso serán de un compuesto de fibra de vidrio y epoxi, con una cara recubierta de cobre, y película de resina fotosensible positiva.

Para atacar el cobre sobrante de las placas se utilizada una solución de cloruro férrico.

La conservación y manejo de las placas de circuito impreso, el proceso de insolado, revelado y atacado de la placa, así como el almacenamiento y manejo de los productos utilizados en cada proceso se ajustara a las normas del fabricante del producto.

La mecanización de las placas de circuito impreso se realizara con brocas de 1mm y 3mm según se especifica en los circuitos impresos.

En caso de duda en el procedimiento a seguir se aplicara la normativa vigente, detalladas en la siguiente secciono

13.4. Normas Generales de Aplicación

Adicionalmente a las condiciones de este pliego, serán de aplicación a este proyecto como normas generales o supletorias las siguientes:

- Reglamento Electrotécnico de Baja Tensión, aprobado por decreto 2414/1973 de Noviembre, B.O.E. 24 de octubre de 1978
- Ordenanza General de Seguridad e Higiene en el Trabajo aprobada por orden ministerial del 9 de Marzo de 1971
- Norma UNE 20512-8:1978, Parte 1, Fiabilidad de equipos y componentes electrónicos, Pequeña introducción sobre la terminología para la resolución de posibles problemas con los términos técnicos.
- Norma UNE 20621-3:1984, Parte 3, Circuitos impresos, Diseño y utilización de placas impresas.
- Norma UNE 20621-3/1C:1985, Parte 3, Primer Complemento, Circuitos impresos
- Norma UNE 20621-5:1985, Parte 5, Circuitos impresos, Especificaciones para placas impresas de simple y doble cara con agujeros metalizados

13.5. Pliego de Condiciones Económicas

Los precios de los materiales que refleja el presupuesto se obtuvieron de tarifas actualizadas a 11 de septiembre de 2003

En el presupuesto se aplica el Impuesto sobre el Valor Añadido (IVA) que en la actualidad es de el 16 % para este tipo de actividad.

El precio total que se ofrece en el presupuesto es el de la realización de un prototipo, En caso de realizarse una producción en serie, los precios variaran debido a reducción de costes en mano de obra y adquisición del material en cantidades.

En caso de que una empresa desee que el proyectista supervise cualquier paso en el proceso de fabricación sera necesario formalizar un contrato donde se especifique el trabajo y competencias del proyectista y las condiciones económicas del servicio.

La validad de la oferta es de tres meses a partir de la fecha de la recepción del proyecto, a 11 de septiembre de 2003. A partir de esa fecha sera necesaria la revisión del presupuesto.

Parte IV

Presupuesto

Tabla de Contenidos

Capítulo 14
Presupuesto

14.1. Coste de Materiales

El coste de los materiales utilizados en el proyecto se ha dividido en dos apartados, por un lado los componentes electrónicos y por otro lado el resto de materiales utilizados en el proyecto

14.1.1. Coste de Materiales Eléctricos

Concepto	P./Unidad	Cantidad	Precio
Placa C.I. 1Cara Posi. 20x30	5		5.00
Par de Sensores de Ultrasonidos	10.35	4	41.40
Cable 4 Hilos	0.34	2	0.68
IC TL81	0.3	4	1.20
IC 40106	0.3	4	1.20
IC PIC 16F84A	15		15.00
IC LM297	4.8		4.80
IC LM7805	0.6		0.60
IC NE555N	0.45	4	1.80
Zócalo 18 pat.	0.36	6	2.16
Zócalo 8 pat	0.22	8	1.76
Cuarzo 4MHz	1		1.00
Condensador 27pf	0.3	2	0.60
Condensador 100nf	0.3		0.30
Condensador 10nf	0.3	8	2.40
Diodo 1N4001	0.03	8	0.24
Diodo 1N4148	0.03	4	0.12
Sigue…			

Concepto	P./Unidad	Cantidad	Precio
Transistor BC549B	0.3	4	1.20
Conector Macho 2	0.64	2	1.28
Conector Hembra 2	0.64	2	1.28
Conector Macho 4	0.82	9	7.38
Conector Hembra 4	0.82	8	6.56
Resistencia 1/4W 47K	0.04	5	0.20
Resistencia 1/4W 1370	0.04	4	0.16
Resistencia 1/4W 230	0.04	4	0.16
Resistencia 1/4W 4.7K	0.04	4	0.16
Resistencia 1/4W 1M	0.04	4	0.16
Potenciómetro C.I. 10K	0.21	4	0.84
Pila Ni-Mh 6F22	15.52		15.52
Pila Ni-Mh AA	2.59	4	10.34
Total			124.74

14.1.2. Coste de Materiales Mecánicos

Concepto	P./Unidad	Cantidad	Precio
Plataforma del Robot en fascículos	5.16	3	15.48
Plancha madera de Ocumen 20x30cm	0.60		0.60
Listón madera de Pino 10x10x200cm	1.00		1.00
Chapa Hierro 105x100x0.5mm 0.50			0.50
Varilla roscada M3	0.50		0.50
Tornillos madera 2cm	0.03	8	0.24
Tornillos M3 5mm	0.03	12	0.36
Tuercas M3	0.03	16	0.48
Separadores de C.I. M3 1/2”	0.05	11	0.55
Total			19.42

14.2. Mano de Obra

14.2.1. Consideraciones

Para la realización del proyecto se han necesitado dos niveles de capacitación diferente, en función de la fase del proyecto, con un coste diferente:

- Precio de trabajo de investigación y desarrollo : 25 Eur./hora.

- Precio de trabajo de Montaje y mecanización : 25 Eur./ hora.

14.2.2. Desglose

Concepto	**Horas**	**Precio**	**Cantidad**
Mano de Obra Ingeniero	352	25	8800
Mano de Obra Ingeniero	56	10	560
Total			9360

14.3. Presupuesto Final

A las cantidades dadas anteriormente se han de añadir:

- Concepto de Gastos generales: 1 %
- Beneficio Industrial : 15 %
- Impuesto sobre el valor añadido: 16 %

Este presupuesto es para la realización de un (1) prototipo del robot, su realización en serie requeriría un estudio de mercado y presupuesto nuevo que se adaptase a las nuevas condiciones.

De acuerdo a lo especificado en el pliego de condiciones, el material electrónico utilizado es fabricado por diferentes firmas comerciales, y su precio y disponibilidad puede variar en función del distribuidor.

Concepto	**Cantidad**
Materiales Eléctricos	124.74
Materiales Mecánicos	19.42
Mano de Obra	9360.00
Subtotal	9504.16
Gastos Generales	95.04
Beneficio Industrial	1425.62
Subtotal	11024.83
IVA	1763.97
Total	12788.80

Asciende el presente presupuesto a la citada cantidad de Doce mil setecientos ochenta y ocho euros con ochenta céntimos de euro.

Oviedo, 11 de septiembre de 2003

Álvaro Alea Fernández

Alumno de la Escuela Universitaria de Ingenieros Técnicos Industriales de Gijón.

Capítulo 15

Viabilidad económica

A continuación se calculara la viabilidad económica del proyecto, así como el numero de unidades necesarias a comercializar para obtener un beneficio económico.

Este calculo es una mera orientación, y en caso de realizar la comercialización requeriría un estudio detallado de mercado.

En el estudio no se han incluido ningún tipo de gastos relacionados con patentes, propiedad intelectual o cualquier otro que fuese necesario para su comercialización.

15.1. Generalidades

Podríamos resumir las características del robot objeto del proyecto en:

1. Robot triciclo con 2 motores para las ruedas.
2. 4 Sensores de Ultrasonidos.
3. Controlado por Microcontrolador PIC de fácil programación por el usuario.

En el mercado es posible conseguir un robot de características similares, partiendo de varios kits:

Microbot Boe-Bot	275.00		275.00
Sensores de Ultrasonidos	22.00	4	88.00
Total			363.00

15.2. Cálculos

Debido a las diferencias de características del robot, un precio de mercado competitivo se situaría en torno a los 275 euros.

El minorista y la red de distribución se llevarían un 20 % siendo el precio con el que se ofrecerla de 220 euros.

Sobre el presupuesto dado anteriormente, hay que añadir unos costes no presupuestados de documentación, embalaje, y otros procesos industriales durante la producción.

3 euros por unidad. 1200 euros por producción.

Los gastos fijos por unidad, están calculados en 147.16 euros.

Los gastos divisibles del proyecto son de 12080.67 euros.

Hay en total de 72.84 euros de margen entre ganancias y costes divisibles.

El robot empezaría a ser comercialmente viable a partir de las 166 unidades.

Se obtendría un 10 % de beneficio a partir de 238 unidades.

Si se construyesen 1000 unidades, el beneficio seria de 27,61 %.

Capítulo 16

Plan de Trabajo

En el proyecto se utilizaron dos recursos humanos

- Un ingeniero
- Un tecnico de FP2

La asignación de las tareas, duraccion y fechas fue la siguiente:

Tarea	Recursos	duración	Fecha inicio	fecha fin
Investigar Sensores	Ingeniero	5	2 Junio	6 Junio
Diseñar C.I. Principal	Ingeniero	3	6 Junio	11 Junio
Diseñar C.I. Sensores	Ingeniero	3	11 Junio	16 Junio
Crear C. Impreso	Tecnico	1	16 Junio	17 Junio
Diseñar Soportes	Ingeniero	2	16 Junio	18 Junio
Crear Soporte Sensores	Tecnico	1	18 Junio	19 Junio
Crear Portapilar	Tecnico	2	19 Junio	23 Junio
Montar el Robot	Tecnico	4	23 Junio	27 Junio
Programar el Pic	Ingeniero	5	18 Junio	25 Junio
Comprobar los C.I.	Ingeniero	3	25 Junio	30 Junio
Comprobar el Programa	Ingeniero	3	30 Junio	3 Julio
Documentación	Ingeniero	20	3 Julio	31 Julio

A continuación se muestra el diagrama de gantt de la planificación del proyecto

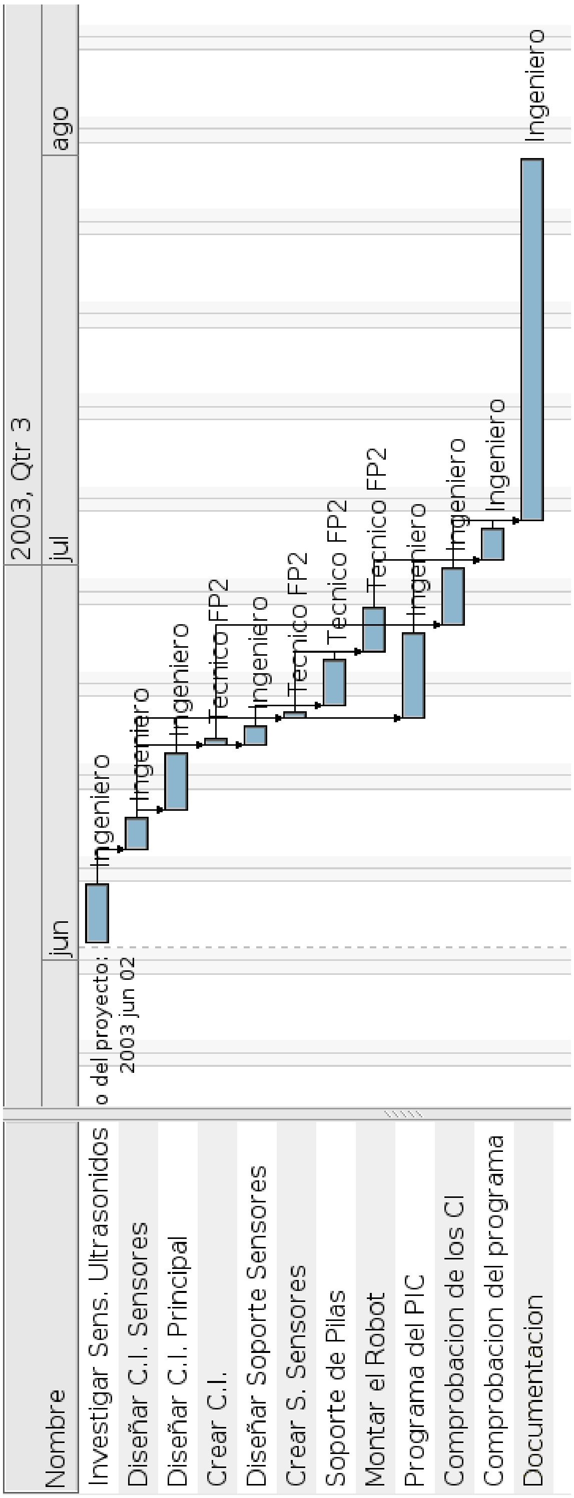


Figura 16.1: Plan de trabajo